100322

100322 Low Power 9-Bit Buffer

Literature Number: SNOS123A

National Semiconductor

100322

OBSOLETE
October 19, 2009

Low Power 9-Bit Buffer

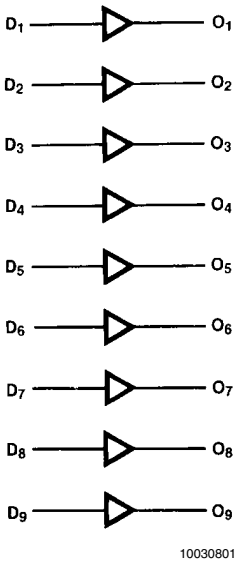
General Description

The 100322 is a monolithic 9-bit buffer. The device contains nine non-inverting buffer gates with single input and output. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Features

- 30% power reduction of the 100122
- 2000V ESD protection
- Pin/function compatible with 100122
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883

Logic Symbol



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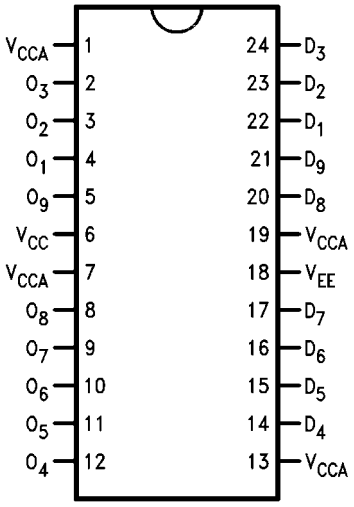
Pin Names	Description
D_1, D_9	Data Inputs
O_1, O_9	Data Outputs

Connection Diagrams

24-Pin DIP



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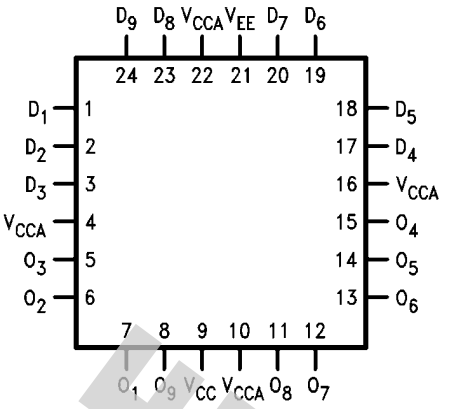
24-Pin Quad Cerpak



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Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impaired.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (*Note 2*)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V	(*Note 3*, *Note 4*, *Note 5*)
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V	(*Note 3*, *Note 4*, *Note 5*)
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		(*Note 3*, *Note 4*, *Note 5*, *Note 6*)
V_{IL}	Input HIGH Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		(*Note 3*, *Note 4*, *Note 5*, *Note 6*)
I_{IL}	Input LOW Current	0.50		µA	−55°C to +125°	V_{EE} = −4.2V V_{IN} = $V_{IL\ (Min)}$		(*Note 3*, *Note 4*, *Note 5*)
I_{IH}	Input HIGH Current		240	µA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = $V_{IH\ (Max)}$		(*Note 3*, *Note 4*, *Note 5*)
			340	µA	−55°C			
I_{EE}	Power Supply Current	−70	−25	mA	−55°C to +125°C	Inputs Open		(*Note 3*, *Note 4*, *Note 5*)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.30	1.80	0.40	1.60	0.40	1.80	ns	Figures 1, 2	(*Note 7*, *Note 8*, *Note 9*, *Note 11*)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.20	0.30	1.20	0.30	1.20	ns		(*Note 10*)

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

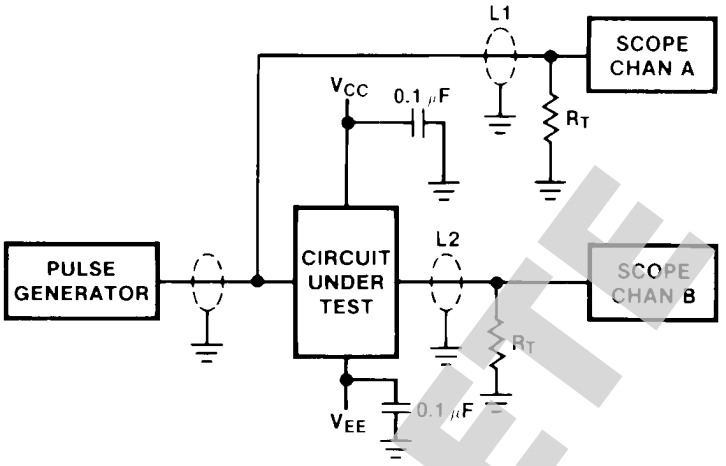
Note 8: Screen tested 100% on each device at +25°C, only Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 10: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 11: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Test Circuit



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Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms

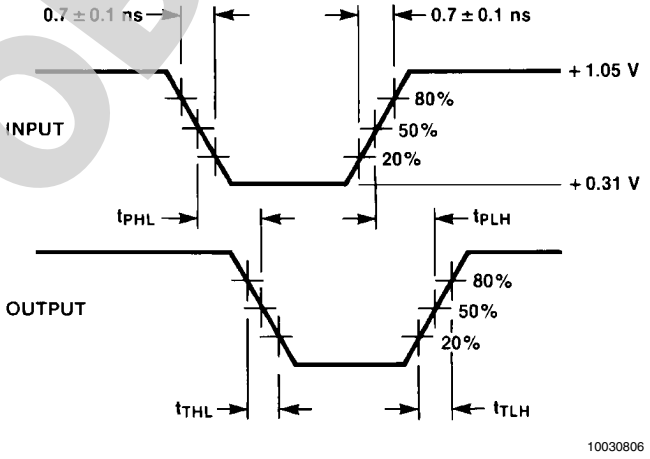

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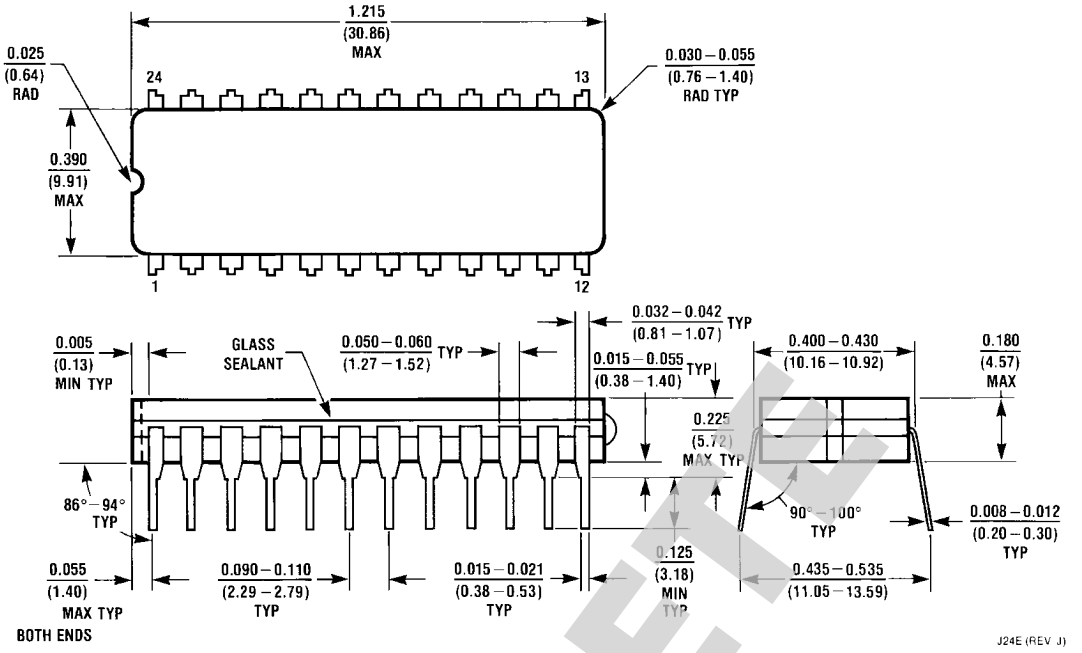
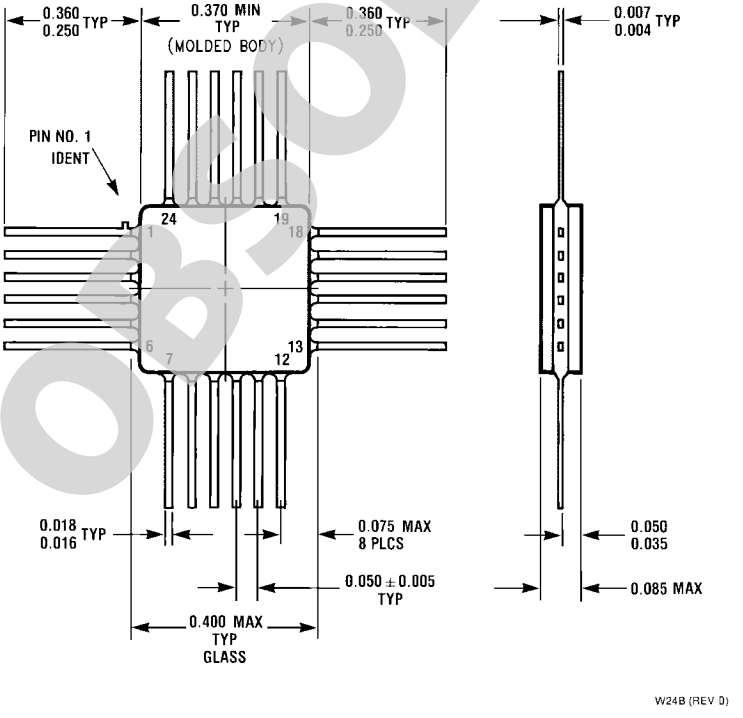
FIGURE 2. Propagation Delay and Transition Times

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



24-Lead Ceramic Flatpak (F)
NS Package Number W24B

Notes

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LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
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