

QUAD 2-INPUT NOR GATE | 10102

10102B,F: -30 to +85°C

DIGITAL 10,000 SERIES ECL

LOGIC DIAGRAM



CIRCUIT SCHEMATIC



FEATURES

DESCRIPTION

• FAST PROPAGATION DELAY = 2.0 ns TYP

current and rise and fall time specifications.

 LOW POWER DISSIPATION = 100 mW/PACKAGE (NO LOAD)

The 10102 is a high speed quad 2-input NOR gate. All

inputs are terminated with a 50 k Ω resistor to VEE which eliminates the need to tie unused inputs low. The gate has an excellent speed-power product of 50 picojoules. The 10102 is optimized for high performance logic applications. This gate meets the ECL 10,000 Series standard voltage

- HIGH FANOUT CAPABILITY
 CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS INTERNAL 50 k Ω PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: VEE = $-5.2 \vee \pm 5\%$ RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

TEMPERATURE RANGE

● _ -30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP F: 16-Pin CERDIP 5-28

LECTRICAL CHARACTERISTICS at Listed Voltages and Ambient Temperatures).											TEST VOLTAGE VALUES (Volts)					
at Listed volta	lent I								VIH max	VIL min	VIHA min	VILA max	VEE			
30°C											-0.890	-1,890	-1.205	-1.500	-5.2	
										+25° C	-0.810	-1.860	-1.105	-1.475	-5.2	1
+85°C										-0.700	-1.825	-1.035	-1,440	-5.2		
Characteristic	Symbol	Pin Under Test	10102 Test Limite								TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					
			-30° C		+25°C			+85°C						·		(Vcc)
			Min	Mex	Min	Тур	Max	Min	Mex	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd -
Power Supply Drein Current	IE.	я	-		-	20	26	-	-	mAde	-	-	~	-	8	1,16
Input Current	linH	12	-	-	-	-	266	-	-	μAde	12	-	-	-	8	1,16
	linL	12	-	-	0.5	-	-	-	-	µAdc		12	-	-	8	1,16
Logic "1" Outout Voltage	VOH	9	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0,700	Vdc	12	-	-	-	8	1,16
	l	9	-1.060	0 890	-0.960	-	-0,810	-0.890	-0.700		13	-	-	- 1		
	1	15	-1.060	-0.890	-0.960	-	-0,810	-0.890	-0.700		-	12	-	-		
		15	-1.060	-0.890	- 0.960	i.	-0.810	-0.890	-0.700		-	13	-	-	1	
Logic "O" Output Voltage	VOL	9	-1.890	-1.675	-1.850	1	-1.660	-1.825	-1.615	Vdc	-	12	-	-	8	1,16
		9	-1.890	-1.675	-1,850	-	-1.650	-1.825	-1.615		-	13	-	-		
	1	16	-1.890	-1.675	-1.860	-	-1.650	-1.826	-1.615		12	-	-	- 1		
		15	-1.890	-1.675	-1.860	-	-1.650	-1.825	-1.615		13	-	-			
Logic "1" Threshold Voltage	VOHA	9	-1.080	-	-0.980	-	-	-0.910	-	Vdc	-	- 1	12	-	8	1,16
		9	-1.080	-	-0.980	-	-	-0.910	-		-	-	13	-		
		15	-1.080	-	-0.980	-	-	-0.910	-		-	-	-	12		
		15	-1.080	-	-0 980	-	-	-0910			-		-	13		
Logic "O" Threshold Vollage	VOLA	9	-	-1.655	-	-	-1.630	-	-1.596	Vdc	-	-	-	12	8	1,16
		9	-	-1.655	-	-	-1.630	-	1.595		-	-	-	13		
		15	- 1	1.665	-	-	-1.630	-	-1.595				12	-		
		15	-	-1.655	-	-	-1,630		-1,696				13			
Switching Times*		Į							ļ]	Puise in	Pulse Out	-3.2 V	+2.0 V
(60 ohm load)												(
Propagation Datay	12+15-	16	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns I	-	-	12	15	8	1,16
	¹ 12-15+	15						11			-	-		15		11
	12+9+	9							-	1	-			9	1 1	
	¹ 12-9	9									-	- 1		9		11
Rise Time (20% to 80%) Fall Time (20% to 90%)	116+	15	1.1	36	1.1		3.3	1.1	3.7		-	-		15		
	19+	9									-	-		9		11
	115-	16								- 12	-	- 1	K. (15	1.1	
	†9 <u>–</u>	9						· ·	1 '	1	- 1	-		9		

*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

- Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltege levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
- 2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
- 3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
- All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.