

DUAL 3-INPUT 1 OR/2 10112 NOR OUTPUT GATE

10112B,F: -30 to +85°C

DIGITAL 10,000 SERIES ECL

LOGIC DIAGRAM



TEMPERATURE RANGE

• -30 to +85°C Operating Ambient

PACKAGE TYPE

- B: 16-Pin Silicone DIP
- F: 16-Pin CERDIP



DESCRIPTION

The 10112 is a dual high speed 3-input 1 OR/2 NOR output gate. The 10112 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire-"OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the 10112 particularly useful in clock distribution applications where minimum clock skew is desired. The 10112 is suitable for use in memory chip select decoding. The 10112 is particularly useful as a clock amplifier on a board using clock signals of both polarities.

FEATURES

- FAST PROPAGATION DELAY = 2.4 ns TYP (ALL OUTPUTS LOADED)
- POWER DISSIPATION = 150 mW/PACKAGE TYP (NO LOAD)
- VERY HIGH FANOUT CAPABILITY – CAN DRIVE SIX 50 Ω LINES
- HIGH Z INPUTS INTERNAL 50 k Ω PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIA-TIONS: VEE = -5.2 V ±5% RECOMMENDED
- OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY

CIRCUIT SCHEMATIC

TEST NOI TAGE WALLIES WA

TEST CONDITIONS

ELECTRICAL CHARACTERISTICS

and I from all \$ do box								@ Test	TE	TEST VOLTAGE VALUES (Volta)					
at Listed Voltages and Ambient Temperatures).								Te	mperature	VIH mex	VIL min	VIHA min	VILA max		
										-30°C	-0.890	-1 890	-1 205	-1.500	1
										+25°C	-0.810	-1.850	-1.105	-1.475	
										+85°C	-0.700	-1.825	-1.035	-1.440	
Characteristic	Symbol	Pin Under Test	10112 Test Limits								TEST VOLTAGE APPLIED TO PINS				
			-30° C		+25°C			+85°C				LISTEC	BELOW		1
			Min	Max	Min	Түр	Мах	Min	Max	Unit	VIH mex	VIL min	VIHA min	VILA max	NOTES
Power Supply Drain Current	1E	8	- 1	-	-	-	38	-	-	mAric	-	-	-	-	5
Input Current	linH	5	_	-	-	-	420	-	-	µAdc	5	-	-	-	5
	linL	5	-	-	0.5		1 million -	-	-	µ Adc	-	5	-	-	5
Logic "1" Output Voltage	VOH	2	-1.060	-0.890	-0.960	-	-0810	-0 890	-0 700	Vdc	5	-	-	-	5
		3	-1.060	· 0.890	-0.960	-	0.810	0 890	-0.700	Vdc	-	6	-	-	6
		4	-1.060	-0 890	-0 960	-	-0.810	-0.890	-0.700	Vdc	-	7	-	-	5
Logic "O" Output Voltage	VOL	2	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	-	5	-		5
		3	-1.890	-1.675	-1,850	-	-1.650	-1.825	-1.615	Vdc	6	- 1	-	-	5
		4	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	7	-	-	-	5
Logic "1" Threshold Voltage	VOHA	2	-1,080	-	-0.980	-	. ÷	-0.910	-	Vdc	-	-	5		5
		3	-1.080	-	-0 980	-	-	-0.910		Vdc	-	-	-	6	5
		4	-1.080	-	-0.980	-	-	-0.910		Vdc	-	-	-	7	5
Logic "O" Threshold Voltage	VOLA	2	-	-1.655		-	-1.650	-	-1.595	Vdc	-	-	-	5	5
		3	-	1.655	+	-	-1.650	-	-1.596	Vdc	-	-	6	-	5
		4	-	-1.655	-	-	-1.660	- 1	-1,695	Vdc	-	-	7	-	5
Switching Times			1										Pulse In	Pulse Out	[
(50 ohm load)															1
Propagation Delay	15+ 2+	2	-	-	1.4	2.4	3.5	-		nş	-	-	5	2	2,6
	^t 5 2	2	-	-	1 1		1 1	-	-		-	-		2	
	15+1-	3	-	-				-			-	-		3	
	t5- 3+	3	-	-				-			-	-		3	
	(5+ 4-	4		-				-	-		-	-		4	
	t5- 4+	4	-	-				-	-		-	-	1 1	4	
Rise Time (20% to 80%)	t2+	2	-		1,1	2.2	3.5	-	-		-	-		2	
	t3+	3	-	-					-		-	-		3	
	14+	4	-	-				- 1	-		-	-		4	
Fall Time (20% to 80%)	12-	2	-	-				-			-	-		2	
	13-	3	-	-	1.1		1.0	-		-	-	-		3	
	14-	4	i -	-	1	1 1	1 1	-		1 1	- 1	-		4	1 1

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

- Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
- 2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
- 3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
- 4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- 5. Pin 1 = Pin 15 = Pin 16 = V_{CC} = 0 V, Pin 8 = V_{EE} = -5.2 V.
- 6. Pin 1 = Pin 15 = Pin 16 = V_{CC} = +2.0 V, Pin 8 = V_{EE} = -3.2 V.