10115B,F: -30 to +85°C

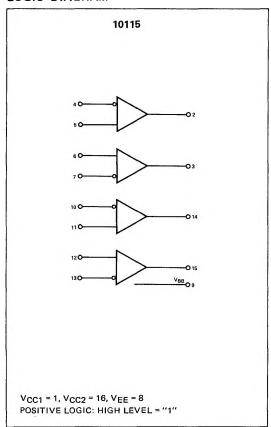
DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10115 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (VBB) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the 10115 with excellent common mode noise rejection. If any amplifier in a package is not used, one input must be connected to VBB (pin 9) to prevent upsetting the current source bias network.

LOGIC DIAGRAM



FEATURES

- GOOD COMMON MODE NOISE REJECTION
- FAST PROPAGATION DELAY = 2.0 ns TYP
- LOW POWER DISSIPATION = 100 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY
 - CAN DRIVE 50 Ω LINES
- HIGH SYSTEM DENSITY FOUR RECEIVERS PER PACKAGE
- VERY HIGH INPUT Z NO 50 K PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIA-TIONS: $V_{EE} = -5.2 \text{ V} \pm 5\% \text{ RECOMMENDED}$
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY
- VBB VOLTAGE AVAILABLE ON PIN 9

TEMPERATURE RANGE

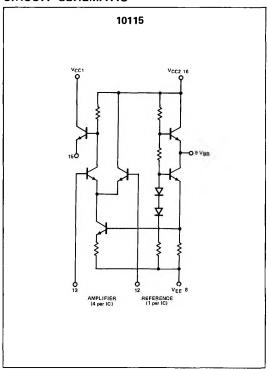
−30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP

F: 16-Pin CERDIP

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

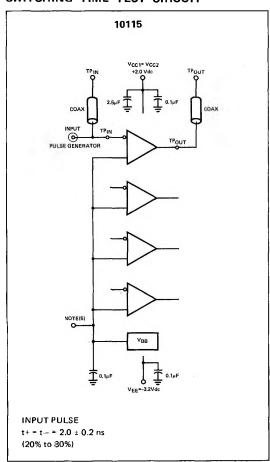
(at Listed Voltages and Ambient Temperatures).

A Yest	TEST VOLTAGE VALUES										
Temperature	VIH max	VIL min	VIHA min	VILA mex	VBB	VEE					
−30° C	-0 890	-1.890	-1.205	-1.500	From	-6.2					
+25° C	- 0.810	-1.860	-1.105	-1.475	Pin	-6.2					
+86°C	-0.700	-1.825	-1.035	-1.440	9	-6.2					

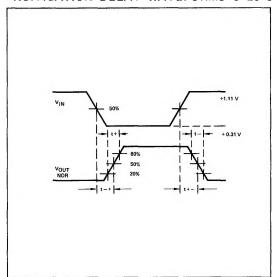
Characteristic	Symbol	Pin Under Test	10115 Test Limits						TEST VOLTAGE APPLIED TO PINS LISTED BELOW:						1	
			-30°C		+25°C		+85°C		T	-	r——	_				IVCCI
			Min	Max	Min	Mex	Min	Mex	Unit	VIH max	VIL min	VIHA min	VILA mex	V _{BB}	VEE	Gnd
Power Supply Drain Current	ΙĘ	8	_	-	-	26	-	-	mAdc	-	4,7,10,13	_	-	5,6,11,12	8	1,16
Input Current	linte	4	-	-	-	95	=	-	μΛdc	4	7,10,13	-		5,6,11,12	8	1,16
-	СВО	4	-	1.5	-	1,0		-	μΛας	-	7,10.13	-	_	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	VOH	2	-1.060	-0 890	-0 960	-0.810	-0.890	-0.700	Vdc	7,10,13	4	-		5,6,11,12	8	1,16
Logic "0" Output Voltage	VOL	2	-1.890	-1.675	-1 850	-1.650	-1.825	-1.615	Vdc	4	7,10,13			5,6,11,12	-8	1,16
Logic "1" Threshold Voltage	VOHA	2	-1.080		-0.980	-	-0,910	-	Vdc	_	7,10,13	-	4	5,6,11,12	8	1,16
Logic "O" Threshold Voltage	VOLA	2	-	-1 655	-	-1.630	-	-1.596	Vdc	-	7,10,13	4		5,6,11,12	8	1,16
Reference Voltage	VBB	9	1,420	1.280	-1.360	-1,230	1.295	-1.150	Vdc	-	-	-		5,6,11,12	-8	1,16
Switching Times * (50 ohm load)		0								Pulse In		Pulse Out			-3.2 V	+2.0 V
Propagation Dalay	14 2+	2	1.0	3,1	1,0	2,9	1,0	3.3	ns	4		13	2 5,6,11,12		8	1,16
	14+ 2-	2	1.0	2.9	1.0	2.9	1,0	3.3						1		1
Rise Time (20% to 80%)	12+	2	1,1	3.6	1.1	3.3	1.1	3.7					Į.	1	1	1
Fell Time (20% to 80%)	12-	2	1.1	3.3	1,1	3.3	1.1	3.7	1				1		1	

^{*}Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES

- 1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
- 2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP $_{\rm in}$ to input pin and TP $_{\rm out}$ to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
- Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
- All voltage measurements are referenced to the ground terminal.
 Terminals not specifically referenced are left electrically open.
- 5. One input from each gate must be tied to $\ensuremath{\text{V}_{BB}}$ (Pin 9) during testing.