

DUAL 2-WIDE 2,3-INPUT 10117 OR-AND/OR-AND-INVERT GATE

10117B,F: -30 to +85°C

DIGITAL 10,000 SERIES ECL

LOGIC DIAGRAM



TEMPERATURE RANGE

● -30 to+85

PACKAGE TYPE

B: 16 Pin Silicone DIP F: 16 Pin CERDIP



DESCRIPTION

The 10117 package contains two 2 input/3 input OR-AND/ OR-AND INVERT complex gates. Pin 9 is common to both gates. This function is particularly useful in data control, multiplexing and distribution. The 10117 is optimized for high performance applications and has an excellent speed power product. All inputs are terminated with a 50 k Ω resistor to VEE which eliminates the need to tie unused inputs low. The high impedance inputs and high output fanout is ideal for a transmission line environment.

FEATURES

- FAST PROPAGATION DELAY FOR TWO LOGIC LEVELS = 2.3 ns TYP
- POWER DISSIPATION = 100 mW/PACKAGE TYP (NO LOAD)
- VERY HIGH FANOUT CAPABILITY - CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIA-TIONS: VEE = -5.2 V ±5% RECOMMENDED
- OPEN EMITTERS FOR BUSSING AND LOGIC CAPABILITY
- OUTPUTS MAY BE CROSS COUPLED BACK TO INPUTS TO MAKE A LATCH FUNCTION

CIRCUIT SCHEMATIC

TEST VOLTAGE VALUES

ELECTRICAL CHARACTERISTICS

at Listed Voltage and Ambient Temperatures).									@ Ten	(Volts)						
										VIH max -0.890	VIL min -1.890 -1.850	VIHA min -1.205 -1.105	VILA max -1.500 -1.475	VEE -6.2 -6.2		
									-30° C							
									+25°C							
		+86°C								-0.700	-1.825	-1.035	-1.440	-5.2		
Characteristic	Symbol	Pin Under Text	10117 Test Limits								TEST VOLTAGE APPLIED TO PINE LIBTED BELOW:					l -
			-30°C		+25°C			+85°C					T	1		(VCC)
			Min	Max	Min	Typ	Max	Min	Mex	Unit	VIH max	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Drain Current	1E -	8	-	-	-	20	26	-	-	mAde	-	-		-	8	1,16
Input Current	linH	4	-	1	+	-	265		-	#Adc	4	-	-	-	8	1,18
		9	-	-	-	-	370	-	-	µAdc	9	-	-	-	8	1,16
	lint	4	-	-	0.5	-	-	-	-	µAdc	-	4			8	1,16
		9	-	-	0.5		-	-	-	µAdc	-	9	-	-	8	1,16
Logic "1" Output Voltage	VOH	2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	4,9	-	-	-	8	1,16
	4.00	3	-1.060	-0.780	-0.960	-	-0.700	-0.890	-0.690	Vdc	-	4,9	-		8	1,16
Logic "0" Output Voltage	VOL	2	-2.000	-1.675	-1.990	-	-1.650	-1.920	-1.616	Vdc	-	4,9	-		8	1,16
		3	-1.890	-1.676	-1.850	-	-1.660	-1.826	-1.615	Vdc	4,9	-	-	-	В	1,16
Logic "1" Threshold Voltage	VOHA	2	-1.080	-	-0.980	-	-	-0.910	-	Vdc	9	1	* 4	-	8	1,16
		3	-1.080	-	-0.980	-	1(-)	-0.910	-	Väc	9	-		4	8	1,16
Logic "0" Threshold Voltage	VOLA	2	-	-1.655			-1.630	1	-1.595	Vdc	9	-	1	- 4	8	1,16
		3		-1.655	-	-	-1.630	-	-1.696	Vdc	9	·	4	-	8	1,16
Switching Times * (50-ohm load)				100			0.22				+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0
Propagation Dalay	14+ 2+	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	9	-	4	2	8	1,16
	14-2-	2	100			1	1	1						2	1.1	
	14+ 3-	3				1.1						-		3		
	14-3+	3	- T	1		1	1	1	1			-		3		
Aise Time (20% to 80%)	12+	2	0.9	4.1	1.1	2.2	4.0	1.1	4.6					2		
	t3+	3				1	1	1 1	1					3		1 1
Fall Time (20% to 80%)	t2-	2				1						1141		2		1.4
	t3_	3				1	1	1 1				-		3		

*Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

- Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
- 2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch⁶ from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
- 3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
- 4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.