

11C06

11C06 750 MHz D-Type Flip-Flop



Literature Number: SNOS372A

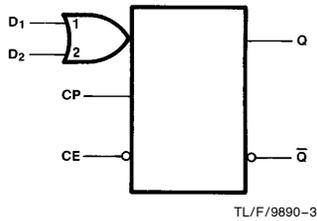
11C06 750 MHz D-Type Flip-Flop

General Description

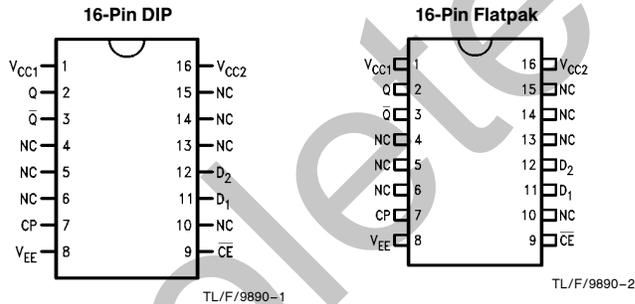
The 11C06 is a high-speed ECL D-Type Master-Slave Flip-Flop capable of toggle rates over 750 MHz. Designed primarily for high-speed prescaling, it can also be used in any application which does not require preset inputs. The circuit is voltage-compensated, which makes input thresholds and

output levels insensitive to V_{EE} variations. Complementary Q and \bar{Q} outputs are provided, as are two Data inputs, Clock and Clock Enable inputs. The 11C06 is pin-compatible with the Motorola MC1690L but is a higher-frequency replacement.

Logic Symbol



Connection Diagrams



Truth Table

Pin Names	Description
D_n	Data Input
CP	Clock Input
\overline{CE}	Clock Enable (Active LOW)
Q, \bar{Q}	Outputs

\overline{CE}	CP	D	Q_n
L	L	X	Q_{n-1}
L	H	X	Q_{n-1}
L	—	L	L
L	—	H	H
H	X	X	Q_{n-1}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
— = LOW to HIGH Transition
 Q_{n-1} = Previous State

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Maximum Junction Temperature (T _J)	+150°C
Supply Voltage Range	-7.0V to GND
Input Voltage (DC)	V _{EE} to GND
Output Current (DC Output HIGH)	-50 mA

Operating Range	-5.7V to -4.7V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max
Supply Voltage (V _{EE})	-5.7V	-5.2V	-4.7V
Ambient Temperature (T _A)	0°C		+75°C

DC Electrical Characteristics

V_{EE} = -5.2V, V_{CC} = GND

Symbol	Parameter	Min	Typ	Max	Units	T _A	Conditions	
V _{OH}	Output Voltage HIGH	-1000		-840	mV	0°C	V _{IN} = V _{IH} (Max) or V _{IL} (Min) per Truth Table Loading 50Ω to -2V	
		-960		-810	mV	+25°C		
		-900		-720	mV	+75°C		
V _{OL}	Output Voltage LOW	-1870		-1635	mV	0°C		
		-1850		-1620	mV	+25°C		
		-1830		-1595	mV	+75°C		
V _{OHC}	Output Voltage HIGH	-1020			mV	0°C	V _{IN} = V _{IH} (Min) or V _{IL} (Max) for D _n Inputs Loading 50Ω to -2V	
		-980			mV	+25°C		
		-920			mV	+75°C		
V _{OLC}	Output Voltage LOW			-1615	mV	0°C		
				-1600	mV	+25°C		
				-1575	mV	+75°C		
V _{IH}	Input Voltage HIGH	-1135		-840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		-1095		-810	mV	+25°C		
		-1035		-720	mV	+75°C		
V _{IL}	Input Voltage LOW	-1870		-1500	mV	0°C		Guaranteed Input Voltage LOW for All Inputs
		-1850		-1485	mV	+25°C		
		-1830		-1460	mV	+75°C		
I _{IH}	Input Current HIGH Clock Input Data Input			250	μA	+25°C	V _{IN} = V _{IH} (Max)	
				270	μA	+25°C		
I _{IL}	Input Current LOW	0.5			μA	+25°C	V _{IN} = V _{IH} (Min)	
I _{EE}	Power Supply Current	-59	-40		mA	+25°C	All Inputs Open	

AC Electrical Characteristics

V_{EE} = -5.2V, V_{CC} = GND, T_A = +25°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t _{PHL}	Propagation Delay (CP-Q)	0.7	1.0	1.2	ns	See Figure 1
t _{PLH}	Propagation Delay (CP-Q)	0.7	1.0	1.2	ns	
t _{TLH}	Transition Time 20% to 80%	0.5	0.8	1.0	ns	
		0.5	0.8	1.0	ns	
t _S	Set-up Time		0.2		ns	
t _H	Hold Time		0.2		ns	
f _{TOG (MAX)}	Toggle Frequency (CP)	650	750		MHz	See Figure 2, Note

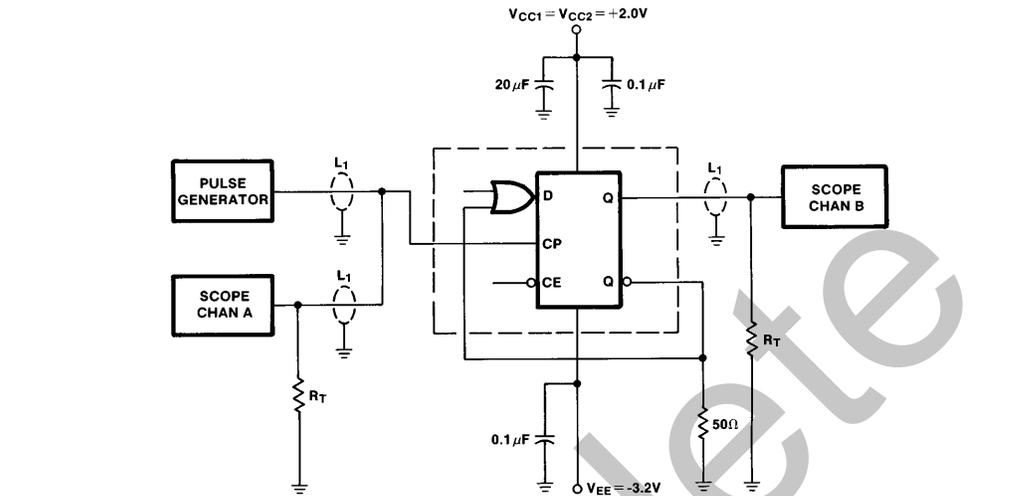
Note: The device is guaranteed for f_{TOG}(CP) ≥ 600 MHz, f_{TOG}(CE) ≥ 550 MHz over the 0°C to +75°C temperature range.

Functional Description

While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous

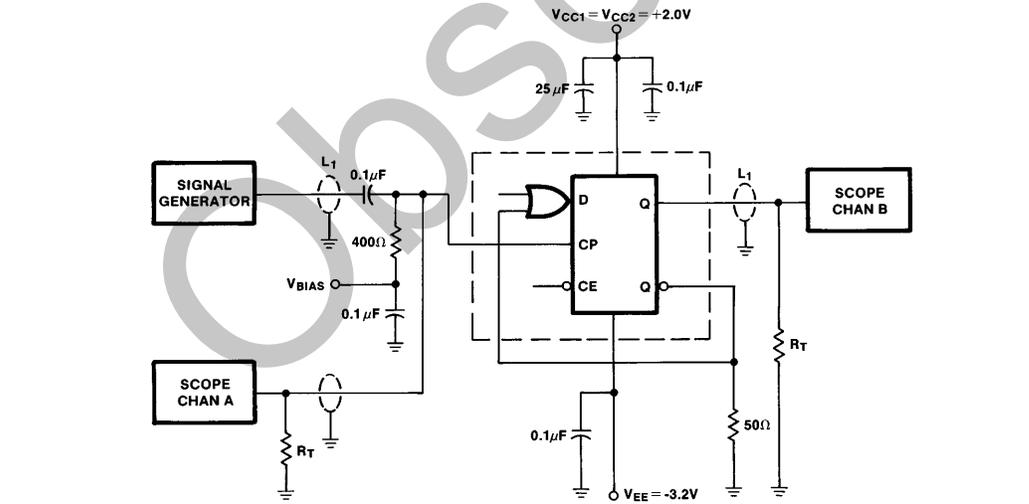
master-slave changes when the clock has slow rise or fall times.

The CP and \overline{CE} inputs are logically identical, but physical constraints associated with the Dual-In-Line package make the \overline{CE} input slower at the upper end of the toggle range. To prevent new data from entering the master on the next CP LOW cycle, \overline{CE} should go HIGH while CP is still HIGH.



$R_T = 50\Omega$ termination of scope
 $L_1 = 50\Omega$ impedance lines
 All input transition times are $2.0\text{ ns} \pm 0.2\text{ ns}$

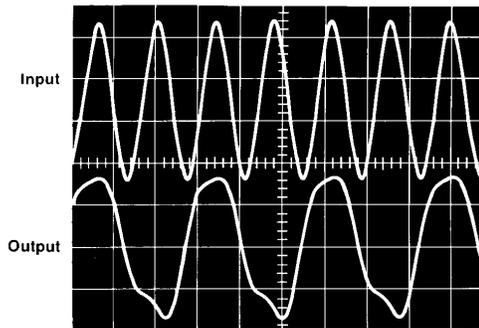
FIGURE 1. Propagation Delay (CP to Q)



$R_T = 50\Omega$ termination of scope
 $L_1 = 50\Omega$ impedance lines
 Adjust V_{BIAS} for $+0.7\text{V}$ baseline of
 800 mV peak-to-peak sinewave input.
 All input transition times are $2.0\text{ ns} \pm 0.2\text{ ns}$

FIGURE 2. Toggle Frequency Test Circuit

Typical Waveforms



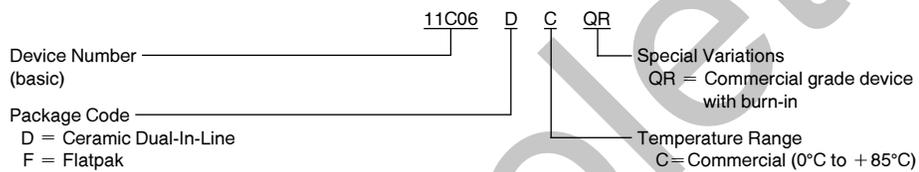
700 MHz Operation

TL/F/9890-6

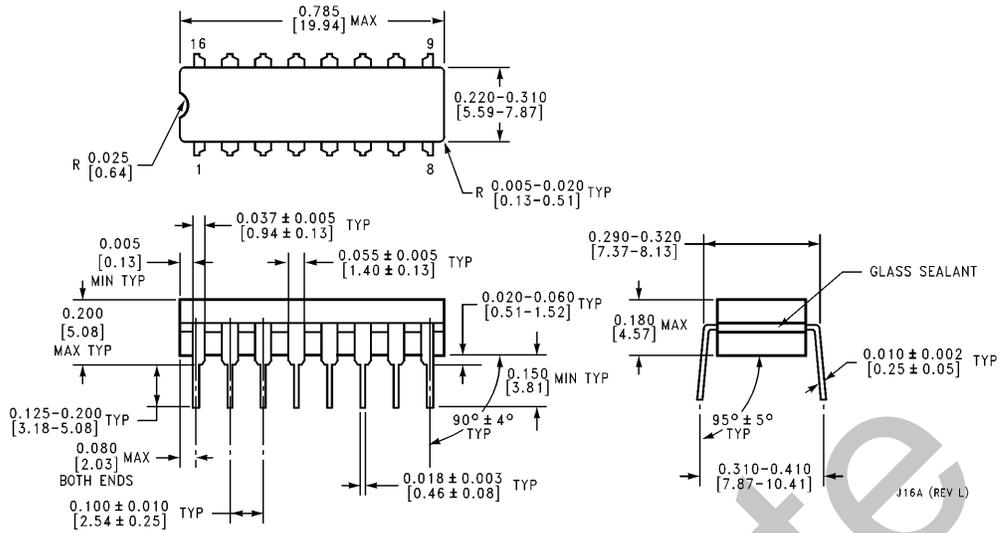
Horizontal Scale = 1.0 ns/div
Vertical Scale = 200 mV/div

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



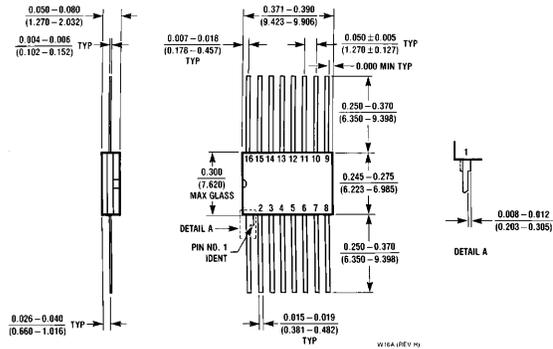
Physical Dimensions inches (millimeters)



**16 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A**

Obsolete

Physical Dimensions inches (millimeters) (Continued)



**16 Lead Ceramic Flatpak (F)
NS Package Number W16A**

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19th Floor, Straight Block,
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