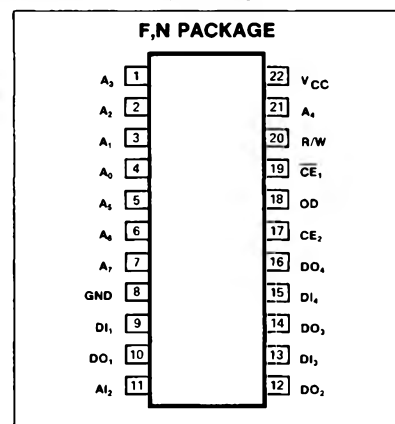


The 2101 series is fabricated with n-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

- **Fully static**
- **No refresh operations, sense amps or clocks required**
- **All inputs and outputs are TTL compatible**
- **One 5V power supply required**

F.N PACKAGE



The logic diagram of the 74VHC163 32x32-bit ROM shows the following components and connections:

- CELL ARRAY:** A 32x32-bit array of memory cells.
- ROW SELECT:** Receives address inputs A_0 through A_7 (pins 4, 3, 2, 1, 21) and controls the row selection of the cell array.
- INPUT DATA CONTROL:** Receives data inputs DI_0 through DI_7 (pins 9, 11, 13, 15) and the read/write control R/W (pin 20). It controls the data flow into the cell array.
- COLUMN I/O CIRCUITS:** Controls the column selection of the cell array.
- COLUMN SELECT:** Receives address inputs A_5 , A_6 , and A_7 (pins 5, 6, 7) and controls the column selection of the cell array.
- Outputs:** Data outputs DO_0 through DO_7 (pins 10, 12, 14, 16) are generated from the cell array.
- Control Logic:**
 - CE_1 (pin 19) and CE_2 (pin 17) are inputs to an AND gate.
 - OD (pin 18) is an input to another AND gate.
 - The outputs of these AND gates are connected to the data outputs DO_0 through DO_7 .
- Power:** V_{CC} (pin 22) and GND (pin 8) are the power supply pins.

PARAMETER		RATING	UNIT
T _A	Temperature range		°C
T _{STG}	Operating under bias	0 to 70	
P _D	Storage	-65 to 150	
	Power dissipation	1	W
	Voltage on any pin with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$, unless otherwise specified

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ²	Max	
V_{IL} Input voltage Low V_{IH} High		-0.5 2.2		0.65 V_{CC}	V
V_{OL} Output voltage Low V_{OH} High	$I_{OL} = 2.0\text{mA}$ $I_{OH} = 150\mu\text{A}$			0.45	V
I_{LI} Input current	$V_{IN} = 0$ to 5.25V			10	μA
I_{LOH} I/O leakage current ³ I_{LOL}	$CE_1 = 2.2\text{V}$ $V_{OUT} = 4.0\text{V}$ $V_{OUT} = 0.45\text{V}$			15 -50	μA
I_{CC1} Supply current I_{CC2}	$V_{IN} = 5.25\text{V}$, $I_O = 0\text{mA}$ $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$		30	60 70	mA
C_{IN} Capacitance ³ Input (All pins) C_{OUT} Output	$V_{IN} = 0\text{V}$ $V_{OUT} = 0\text{V}$		4 8	8 12	pF

AC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$, Input pulse levels = $+0.65\text{V}$ to 2.2V , Input pulse rise and fall times = 20ns , Timing measurement reference level = 1.5V , Output load = 1 TTL gate and $C_L = 100\text{pF}$, unless otherwise specified.

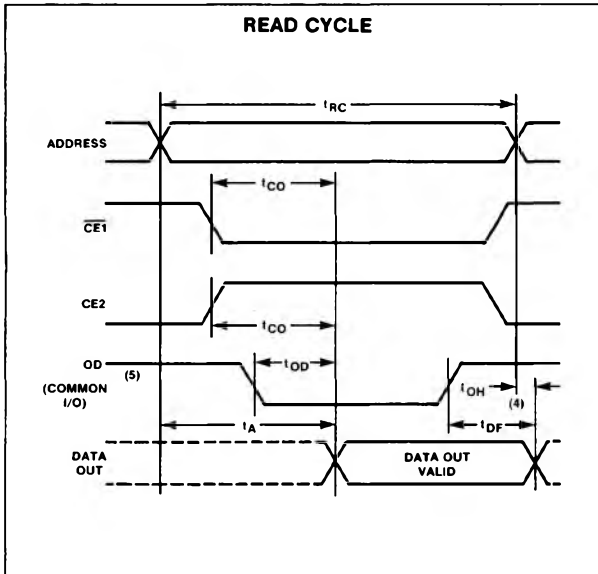
PARAMETER	TO	FROM	2101			2101-1			2101-2			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RC} READ CYCLE Read cycle t_A Access time			1,000			500			650			ns
t_{CO}	Output	Chip enable			1,000			500			650	ns
t_{OD}	Output	Output disable			800			350			400	ns
t_{DF}^4	High Z state	Data output			700			300			350	ns
t_{OH}			0		200	0		150	0		150	ns
	Previous read data valid after change of address		40			40			40			ns
t_{WC} WRITE CYCLE Write cycle t_{AW} Write delay t_{CW}			1,000			500			650			ns
			150			100			150			ns
	Write	Chip enable	900			400			550			ns
t_{DW} Setup and hold time Setup time t_{DH} Hold time			700			280			400			ns
	Rise of R/W	Data in				100			100			
t_{DS} Setup time	Change of data in	Rise of R/W										
	Output	Output disable	200			150			150			
t_{WP} Write pulse t_{WR} Write recovery			750			300			400			ns
			50			50			50			ns

NOTES

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Typical values are for $T_A = 25^\circ\text{C}$ and typical supply voltage.
- This parameter is periodically sampled and is not 100% tested.
- t_{OF} is with respect to the trailing edge of CE_1 , CE_2 or OD , whichever occurs first.
- CD should be tied low for separate I/O operation.

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE

