2101-F,N • 2101-1-F,N • 2101-2-F,N

DESCRIPTION

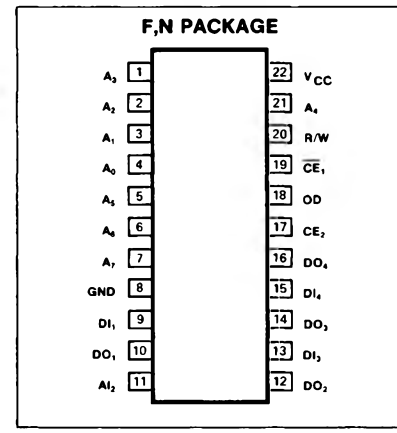
The 2101 series is high performance, low power static read/write RAM's.

The 2101 series is fabricated with n-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

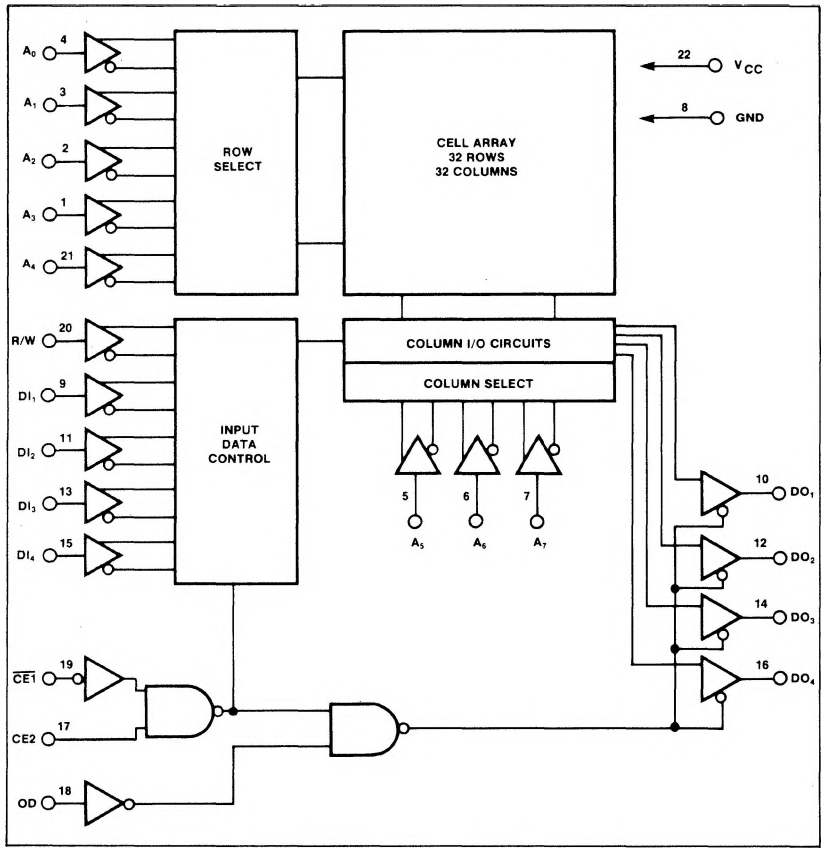
FEATURES

- **Fully static**
- **No refresh operations, sense amps or clocks required**
- **All inputs and outputs are TTL compatible**
- **One 5V power supply required**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.65	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.0mA			0.45	
V_{OH}	High	I_{OH} = 150μA	2.2			
I_{LI}	Input current	V_{IN} = 0 to 5.25V			10	μA
	I/O leakage current[3]	$\overline{CE_1}$ = 2.2V				μA
I_{LOH}		V_{OUT} = 4.0V			15	
I_{LOL}		V_{OUT} = 0.45V			-50	
	Supply current	V_{IN} = 5.25V, I_O = OmA				mA
I_{CC1}		T_A = 25°C		30	60	
I_{CC2}		T_A = 0°C			70	
	Capacitance[3]					pF
C_{IN}	Input (All pins)	V_{IN} = 0V		4	8	
C_{OUT}	Output	V_{OUT} = 0V		8	12	

AC ELECTRICAL CHARACTERISTICS

T_A =0°C to 70°C, V_{CC} = 5V ± 5%, Input pulse levels = +0.65V to 2.2V, Input pulse rise and fall times = 20ns, Timing measurement reference level = 1.5V, Output load = 1 TTL gate and C_L = 100pF, unless otherwise specified.

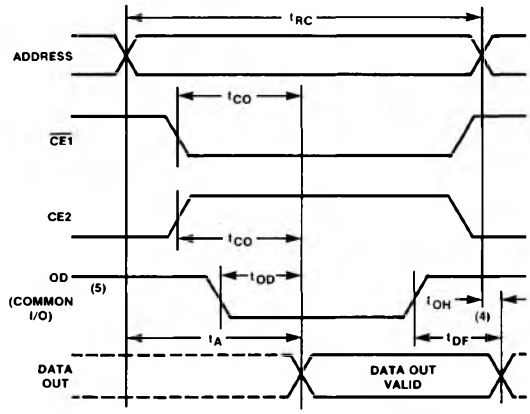
PARAMETER		TO	FROM	2101			2101-1			2101-2			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ CYCLE												
t_{RC}	Read cycle			1,000			500			650			ns
t_A	Access time					1,000			500			650	ns
t_{CO}		Output	Chip enable			800			350			400	ns
t_{OD}		Output	Output disable			700			300			350	ns
t_{DF}[4]		High Z state	Data output	0		200	0		150	0		150	ns
t_{OH}	Previous read data valid after change of address			40			40			40			ns
	WRITE CYCLE												
t_{WC}	Write cycle			1,000			500			650			ns
t_{AW}	Write delay			150			100			150			ns
t_{CW}		Write	Chip enable	900			400			550			ns
	Setup and hold time												ns
t_{DW}	Setup time	Rise of R/W	Data in	700			280			400			
t_{DH}	Hold time	Change of data in	Rise of R/W	100			100			100			
t_{DS}	Setup time	Output	Output disable	200			150			150			
t_{WP}	Write pulse			750			300			400			ns
t_{WR}	Write recovery			50			50			50			ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated In the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25°C and typical supply voltage.
3. This parameter is periodically sampled and is not 100% tested.
4. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, CE_2 or OD, whichever occurs first.
5. CD should be tied low for separate I/O operation.

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE