2107B
4096 BIT DYNAMIC RAM

	2107B	2107B-4	2107B-5
Access Time	200ns	270ns	300ns
Read,Write Cycle	400ns	470ns	590ns
RMW Cycle	520ns	590ns	750ns

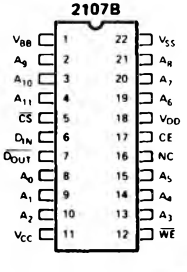
- **Low Cost Per Bit**
- **Low Standby Power**
- **Easy System Interface**
- **Only One High Voltage Input Signal — Chip Enable**
- **TTL Compatible — All Address, Data, Write Enable, Chip Select Inputs**
- **Refresh Period—2ms for 2107B, 2107B-4, 1ms for 2107B-5 @70°C**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion — Chip Select Input Lead**
- **Fully Decoded — On Chip Address Decode**
- **Output is Three State and TTL Compatible**
- **Industry Standard 22-Pin Configuration**

The Intel®2107B is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 2107B uses dynamic circuitry which reduces the standby power dissipation.

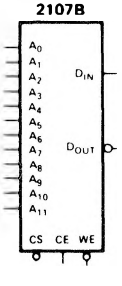
Reading information from the memory is non-destructive. Refreshing is most easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107B is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies. The 2107B uses a single transistor cell to achieve high speed and low cost. It is a replacement for the 2107A.

PIN CONFIGURATION



LOGIC SYMBOL

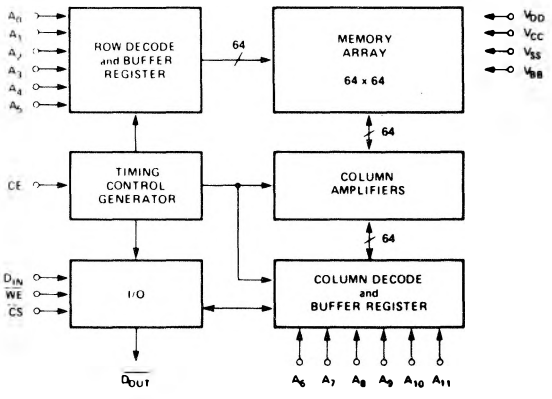


PIN NAMES

A_0-A_{11}	ADDRESS INPUTS*	V_{BB}	POWER (-5V)
CE	CHIP ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	V_{DD}	POWER (+12V)
D_{IN}	DATA INPUT	V_{SS}	GROUND
$\overline{D_{OUT}}$	DATA OUTPUT	$\overline{WE}$	WRITE ENABLE
NC	NOT CONNECTED		

*Refresh Address A_0-A_5.

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +150°C

All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} . . . . . +25V to −0.3V

Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} . . . . . +20V to −0.3V

Power Dissipation 1.25W

*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±10%, V_{BB} [1] = −5V ±5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}[6]	Input Load Current (all inputs except CE)		.01	50	µA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$ CE = V_{ILC} or V_{IHC}
I_{LC}	Input Load Current		.01	2	µA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state		.01	10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		110	200[5]	µA	CE = -1V to +.6V
I_{DD2}	V_{DD} Supply Current during CE on			60	mA	CE = V_{IHC}, $\overline{CS}$ = V_{IL}
$I_{DD\ AV}$	Average V_{DD} Current		38	54	mA	$\overline{CS}$ = V_{IL} ; T_A = 25°C; Min cycle time, Min t_{CE}
I_{CC1}[4]	V_{CC} Supply Current during CE off		.01	10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
I_{BB}	V_{BB} Supply Current		5	400	µA	
V_{IL}	Input Low Voltage	-1.0		0.6	V	t_T = 20ns, V_{ILC} = +1.0V
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	t_T = 20ns
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD}-1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -2.0mA

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V or more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.
5. Maximum I_{DD1} for 2107B-5 is 250 µA.
6. During CE high a current of 0.5mA typical, 1.5mA maximum will be drawn from any address pin which is switched from low to high.

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	2107B		2107B-4		2107B-5		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Time Between Refresh		2		2		1	ms	7
t_{AC}	Address to CE Set Up Time	0		0		10		ns	3
t_{AH}	Address Hold Time	100		100		100		ns	
t_{CC}	CE Off Time	130		130		200		ns	
t_T	CE Transition Time	10	40	10	40	10	40	ns	
t_{CF}	CE Off to Output High Impedance State	0		0		0		ns	

READ CYCLE

Symbol	Parameter	2107B		2107B-4		2107B-5		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	400		470		590		ns	4
t_{CE}	CE On Time	230	4000	300	4000	350	3000	ns	
t_{CO}	CE Output Delay		180		250		280	ns	5
t_{ACC}	Address to Output Access		200		270		300	ns	6
t_{WL}	CE to $\overline{WE}$	0		0		0		ns	
t_{WC}	$\overline{WE}$ to CE On	0		0		0		ns	

WRITE CYCLE

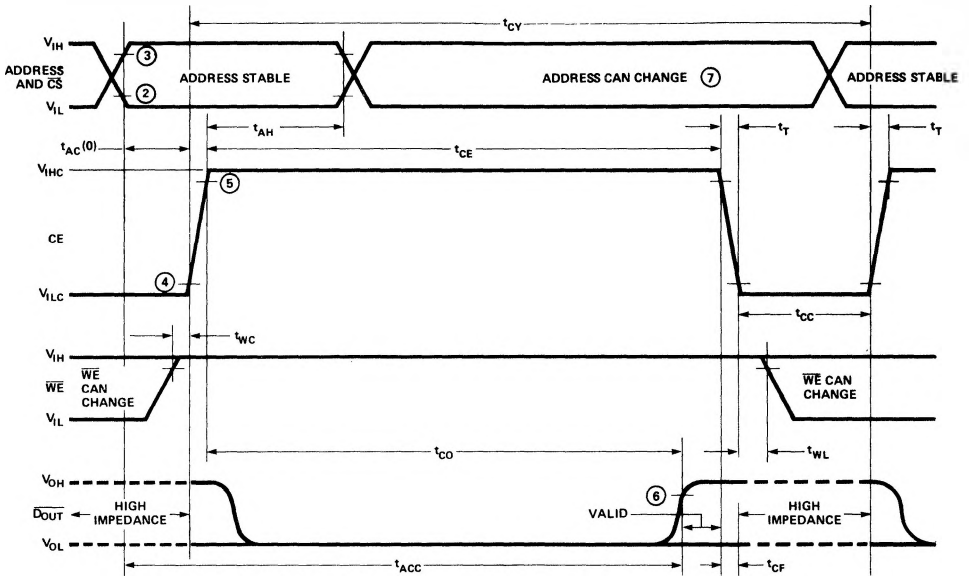
Symbol	Parameter	2107B		2107B-4		2107B-5		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	400		470		590		ns	4
t_{CE}	CE On Time	230	4000	300	4000	350	3000	ns	
t_W	$\overline{WE}$ to CE Off	125		150		200		ns	
t_{CW}	CE to $\overline{WE}$	150		150		150		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		0		0		ns	1
t_{DH}	D_{IN} Hold Time	0		0		0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		50		75		ns	
t_{WW}	$\overline{WE}$ Delay	75		75		75		ns	

Capacitance[2] $T_A = 25°C$

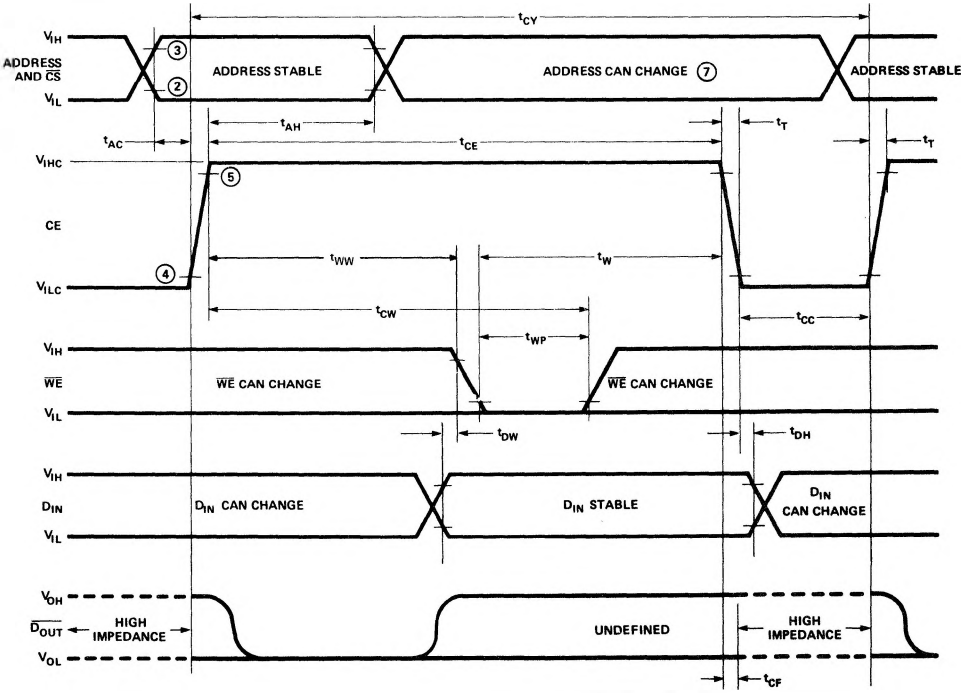
Symbol	Test	Plastic And Ceramic Pkg. Typ.	Max.	Unit	Conditions
C_{AD}	Address Capacitance, $\overline{CS}$	4	6	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	17	25	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	5	7	pF	$V_{OUT} = 0V$
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	8	10	pF	$V_{IN} = V_{SS}$

Notes:
1. If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.
2. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation.
   $C = \frac{I\Delta t}{\Delta V}$ with the current equal to a constant 20mA.
3. t_{AC} is measured from end of address transition.
4. $t_T = 20ns$
5. $C_{LOAD} = 50pF$, Load = One TTL Gate, Ref = 2.0V.
6. $t_{ACC} = t_{AC} + t_{CO} + 1t_T$
7. $t_{REF} = 2ms$ at $T_A = 55°$ C for the 2107B-5.

Read and Refresh Cycle [1]



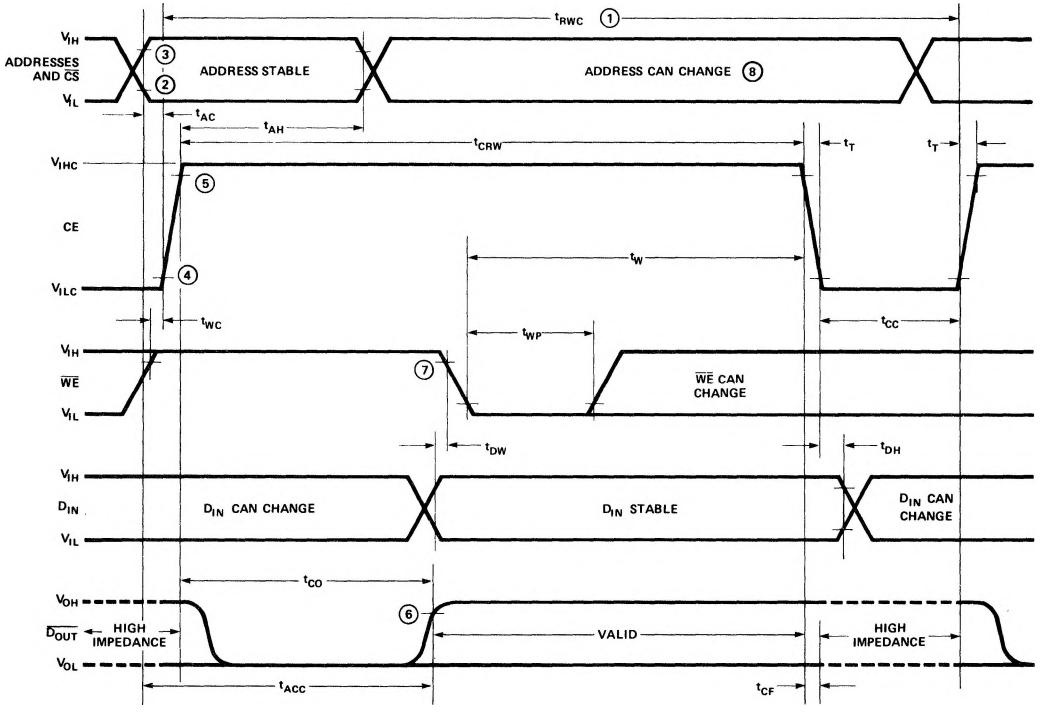
Write Cycle



NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Read Modify Write Cycle[1]

Symbol	Parameter	2107B		2107B-4		2107B-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RWC}	Read Modify Write (RMW) Cycle Time	520		590		750		ns
t_{CRW}	CE Width During RMW	350	4000	420	4000	510	3000	ns
t_{WC}	$\overline{WE}$ to CE on	0		0		0		ns
t_W	$\overline{WE}$ to CE off	150		150		200		ns
t_{WP}	$\overline{WE}$ Pulse Width	50		50		100		ns
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		0		0		ns
t_{DH}	D_{IN} Hold Time	0		0		0		ns
t_{CO}	CE to Output Delay		180		250		280	ns
t_{ACC}	Access Time ($t_{ACC} = t_{AC} + t_{CO} + 1t_T$)		200		270		300	ns



NOTES:
1. Minimum cycle timing is based on t_T of 20ns.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$. C_{LOAD} = 50pF. Load = One TTL Gate.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.
8. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Typical Characteristics

Fig. 1. I_{DD} AV VS. TEMPERATURE

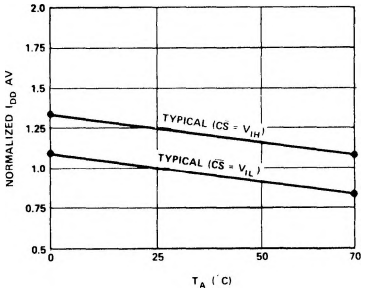


Fig. 2. TYPICAL I_{DD} AVERAGE VS. CYCLE TIME

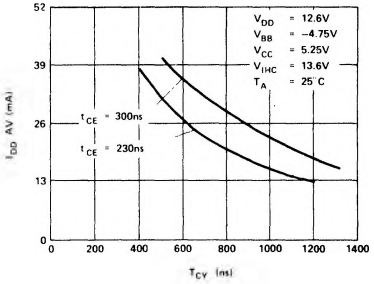


Fig. 3. I_{DD2} VS. TEMPERATURE

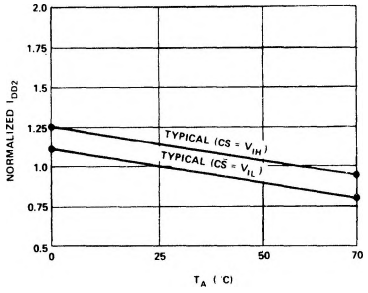
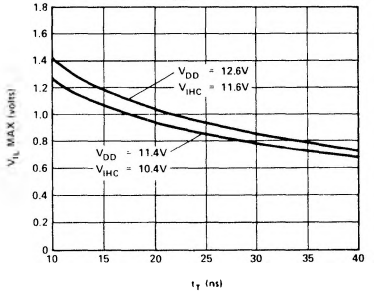
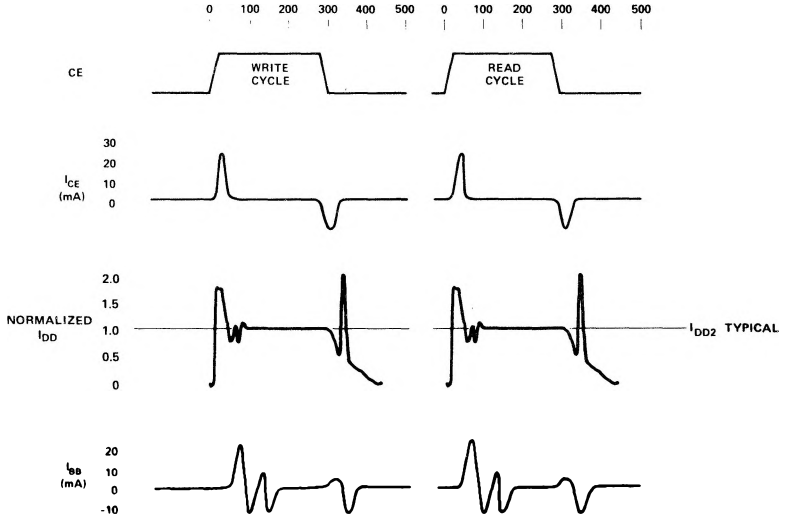


Fig. 4. TYPICAL V_{IL} MAX VS. CE RISE TIME



Typical Current Transients vs. Time



For additional typical characteristics and applications information please refer to Intel Application Note AP-10, "Memory System Design With the Intel 2107B 4K RAM" or Intel's Memory Design Handbook.