2112-F,N • 2112-1-F,N • 2112-2-F,N

DESCRIPTION

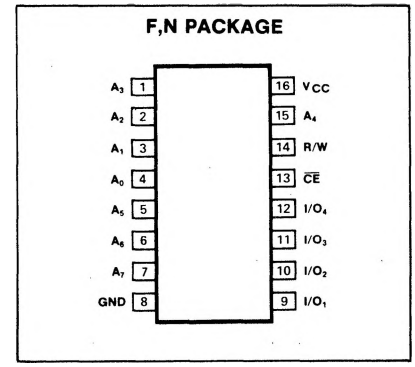
The 2112 series is high performance, low power static read/write RAMs.

The 2112 series is fabricated with n-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

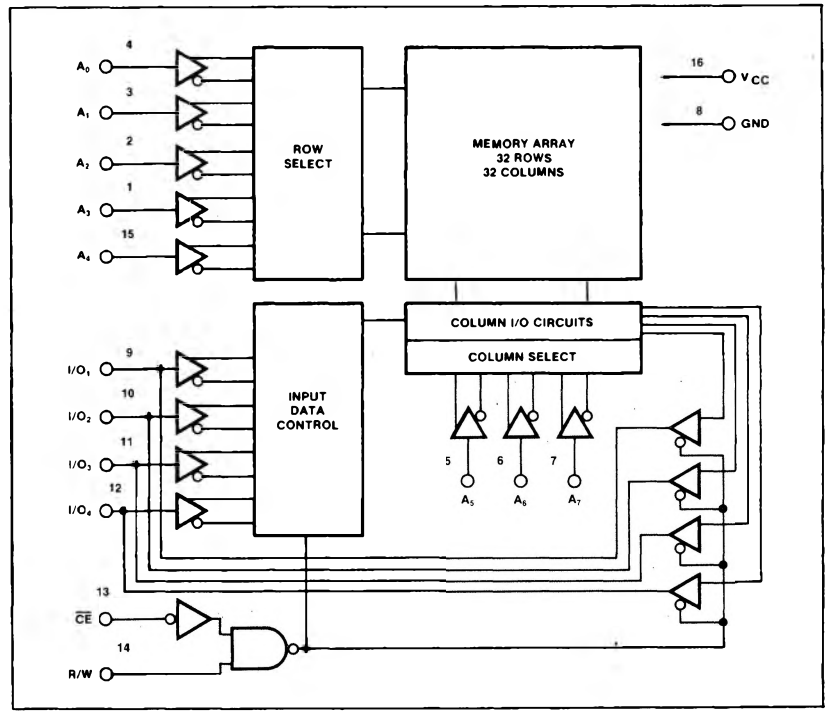
FEATURES

- **Fully static**
- **No refresh operations, sense amps or clocks required**
- **Directly TTL compatible**
- **One 5V power supply**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	0 to 70	
T_{STG}	Storage	-65 to 150	
	Voltage on any pin with respect to ground	-0.5 to 7	V
P_D	Power dissipation	1	W

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.65	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2mA			0.45	
V_{OH}	High	I_{OH} = -150μA	2.2			
I_{LI}	Input current	V_{IN} = 0 to 5.25V			10	μA
	I/O leakage current	$\overline{CE}$ = 2.2V				μA
I_{LOH}		$V_{I/O}$ = 4.0V			15	
I_{LOL}		$V_{I/O}$ = 0.45V			-50	
	Supply current	V_{IN} = 5.25V, $I_{I/O}$ = 0mA				mA
I_{CC1}		T_A = 25°C		30	60	
I_{CC2}		T_A = 0°C			70	
	Capacitance[3]	T_A = 25°C, f = 1MHz				pF
C_{IN}	Input (All pins)	V_{IN} = 0V		4	8	
$C_{I/O}$	I/O	$V_{I/O}$ = 0V		10	15	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified,
t_R and t_F = 20ns, V_{IN} = 0.65V to 2.2V, Timing reference = 1.5V,
Load = 1 TTL gate and C_L = 100pF

PARAMETER		TO	FROM	2112			2112-1			2112-2			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ CYCLE												
t_{RC}	Read cycle			1000			500			650			ns
t_A	Access time					1000			500			650	ns
t_{CO}		Output	Chip enable			800			150			500	ns
t_{CD}		Output disable	Chip enable	0		200	0		100	0		150	ns
t_{OH}	Previous read data valid after change of address			40			40			40			ns
	WRITE CYCLE #1												
t_{WC1}	Write cycle			850			500			500			ns
	Setup and hold time												ns
t_{AW1}	Setup time	Write	Address	150			100			100			
t_{DW1}	Setup time	R/W high	Data	650			250			280			
t_{CS1}	Setup time	$\overline{CE}$ low	R/W low	0			0			0			
t_{CH1}	Hold time	$\overline{CE}$ high	R/W high	0			0			0			
t_{DH1}	Hold time	Data	R/W high	100			50			50			
t_{CW1}	Setup time	R/W high	$\overline{CE}$ low	650			250			350			
t_{WP1}	Write pulse width			650			250			350			ns
t_{WR1}	Write recovery time			50			50			50			ns
	WRITE CYCLE #2												
t_{WC2}	Write cycle			1050			500			650			ns
	Setup and hold time												ns
t_{AW2}	Setup time	Write	Address	150			100			100			
t_{DW2}	Setup time	R/W high	Data	650			250			280			
t_{CS2}	Setup time	$\overline{CE}$ low	R/W low	0			0			0			
t_{CH2}	Hold time	$\overline{CE}$ high	R/W high	0			0			0			
t_{DH2}	Hold time	Data	R/W high	100			50			50			
t_{WD2}	Disable time	R/W high	Data	200			200			200			ns
t_{WR2}	Write recovery time			50			50			50			ns

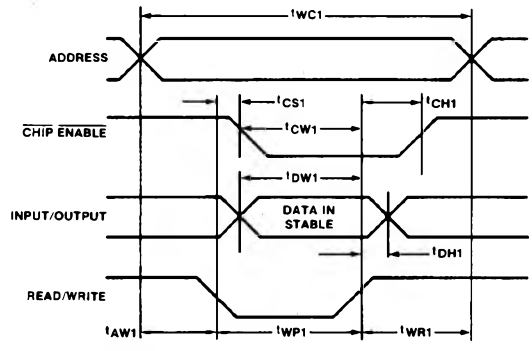
NOTES on following page.

NOTES

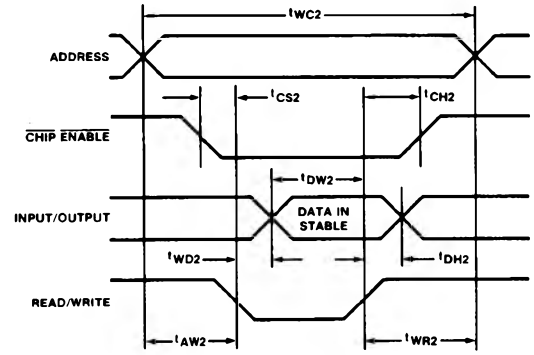
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25° C and typical supply voltage.
3. This parameter is periodically sampled and is not 100% tested.
4. Output is enabled and t_{CO} commences only with both CE low and WE high.
5. Output is disabled and t_{DF} combined from either the rising edge of CE or the falling edge of WE.
6. Minimum t_{WP} is valid when CE has been high at least t_{DF} before WE goes low. Oherwise $t_{WP(min)} = t_{DW(min)} + t_{DF(max)}$.
7. When WE goes high at the end of the write cycle, it will be possible to turn on the output buffers if CE is still low. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.

VOLTAGE WAVEFORMS

WRITE CYCLE #1



WRITE CYCLE #2



READ CYCLE