PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

2114
1024 X 4 BIT STATIC RAM

	2114-2	2114-3	2114	2114L3	2114L
Max. Access Time (ns)	200	300	450	300	450
Max. Power Dissipation (mw)	710mw	710mw	710mw	370mw	370mw

- **High Density 18 Pin Package**
- **Identical Cycle and Access Times**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **Pin-Out Compatible with 3605 and 3625 Bipolar PROMs**

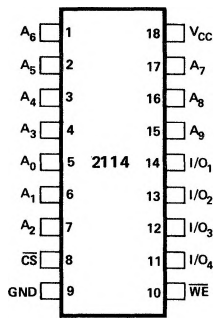
The Intel® 2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The 2114 is placed in an 18-pin package for the highest possible density.

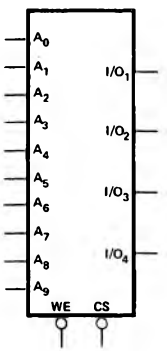
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

The 2114 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

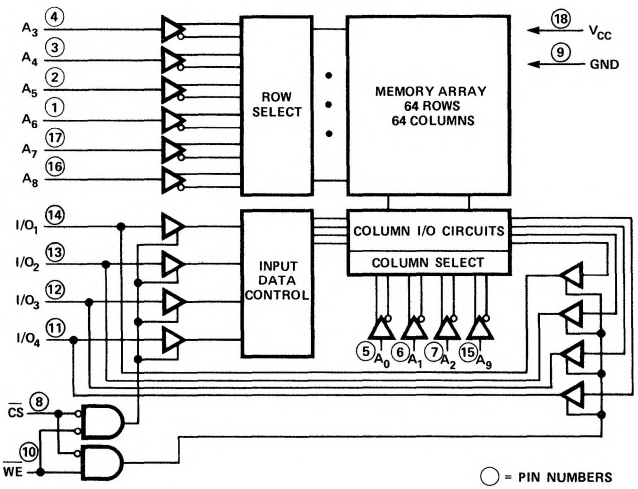
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . -0.5V to +7V
Power Dissipation 1.0W

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.

SYMBOL	PARAMETER	2114-2, 2114-3, 2114 Min.	Typ.	Max.	2114L3, 2114L Min.	Typ.	Max.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)			10			10	μA	V_{IN} = 0 to 5.25V
$\|I_{LO}\|$	I/O Leakage Current			10			10	μA	$\overline{CS}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		80	120			65	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current		90	135			70	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}	2.4		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V_{CC}	2.4		V_{CC}	V	I_{OH} = -1.0 mA

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = OV
C_{IN}	Input Capacitance	5	pF	V_{IN} = OV

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise noted.

READ CYCLE [1]

SYMBOL	PARAMETER	2114-2 Min.	2114-2 Max.	2114-3, 2114L3 Min.	2114-3, 2114L3 Max.	2114, 2114L Min.	2114, 2114L Max.	UNIT
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{CO}	Chip Selection to Output Valid		70		100		100	ns
t_{CX}	Chip Selection to Output Active	0		0		0		ns
t_{OTD}	Output 3-state from Deselection	0	40	0	80	0	100	ns
t_{OHA}	Output Hold from Address Change	10		10		10		ns

WRITE CYCLE [2]

SYMBOL	PARAMETER	2114-2 Min.	2114-2 Max.	2114-3, 2114L3 Min.	2114-3, 2114L3 Max.	2114, 2114L Min.	2114, 2114L Max.	UNIT
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Time	100		150		200		ns
t_{WR}	Write Release Time	20		0		0		ns
t_{OTW}	Output 3-state from Write	0	40	0	80	0	100	ns
t_{DW}	Data to Write Time Overlap	100		150		200		ns
t_{DH}	Data Hold From Write Time	0		0		0		ns

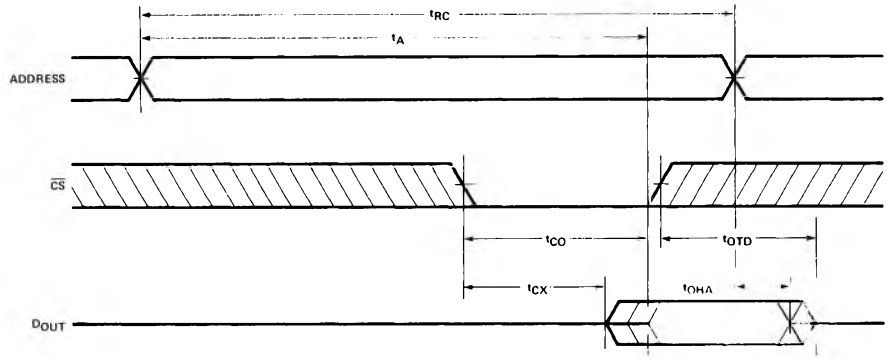
NOTES: 1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

A.C. CONDITIONS OF TEST

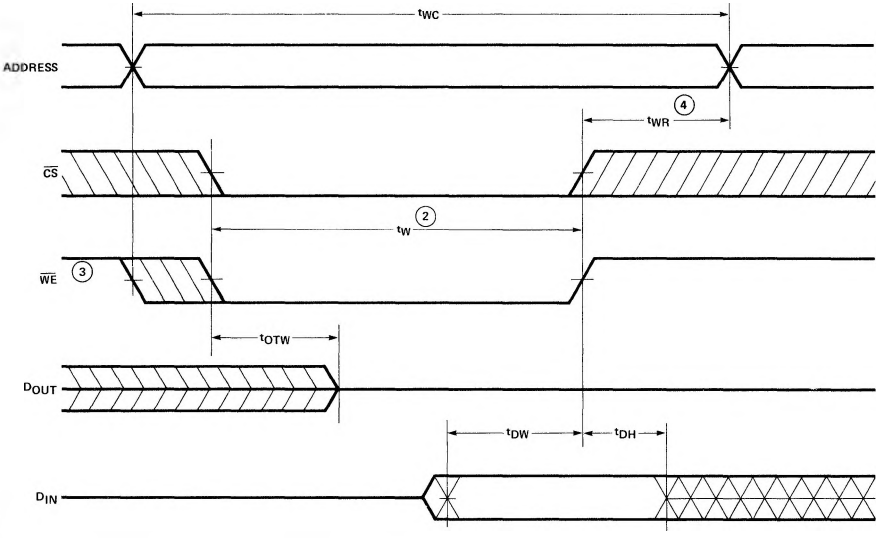
Input Pulse Levels . . . . . 0.8 Volt to 2.4 Volt
Input Rise and Fall Times . . . . . 10 nsec
Input and Output Timing Levels . . . . . 1.5 Volts
Output Load . . . . . 1 TTL Gate and C_L = 50 pF

WAVEFORMS

READ CYCLE ①



WRITE CYCLE



NOTES:
① $\overline{WE}$ is high for a Read Cycle.
② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to $\overline{WE}$ going high.
③ $\overline{WE}$ must be high during all address transitions.
④ t_{WR} is referenced to the high transition of $\overline{WE}$.

DATA STORAGE

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{WE}$ remains high, the data stored cannot be affected by the address, Chip Select, or data I/O voltage levels and timing transitions. The block diagram also shows data storage cannot be affected by $\overline{WE}$, the addresses, nor the I/O ports as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ by itself — or in conjunction with the other — can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during a Write time — defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. To prevent the loss of data, the addresses must be properly established during the entire Write time plus t_{WR}.

Internal delays on the 2114 are established such that address decoding propagates ahead of data inputs (keyed by the Write time). Therefore, it is permissable to establish the addresses coincident to the selection of a Write time, but no later. If the Write time precedes the addresses, the data in the previously addressed locations, or some other location, may be inadvertently changed.

While it is important that the addresses remain stable for the entire Write cycle, the data inputs are not required to remain stable. Appropriate voltage levels will be written into the cells as long as the data is stable for t_{DW} at the end of the Write time.