

# 1024-BIT READ/WRITE STATIC MOS RAM (1024X1) 21L02/21L02-1/21L02-2/21L02-3

21L02-F,I,N • 21L02-1-F,I,N • 21L02-2-F,I,N • 21L02-3-F,I,N

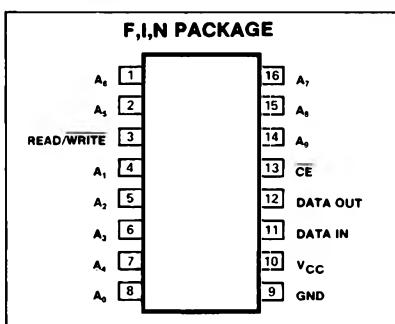
## DESCRIPTION

The 21L02, 21L02-1, 21L02-2, and 21L02-3 are low power static random access read/write memories fabricated with low threshold n-channel silicon gate technology.

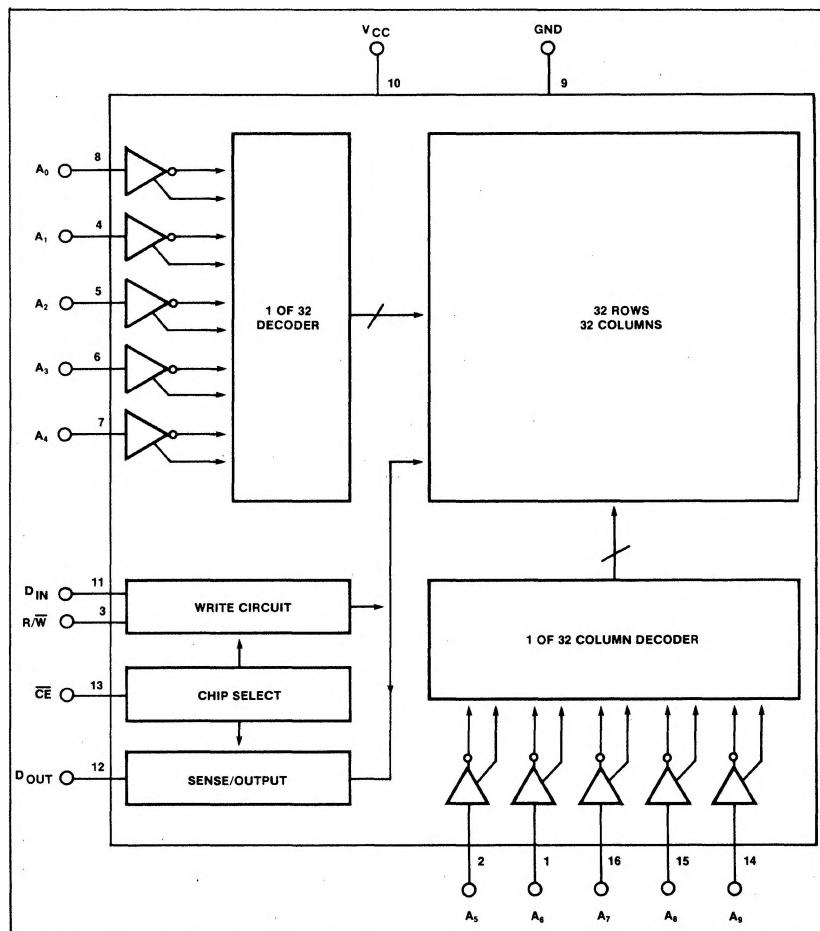
## FEATURES

- Fully static
- Requires no clocks
- Completely DTL/TTL compatible
- Single 5V power supply
- Three-state output for OR-tie capability

## PIN CONFIGURATION



## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

PARAMETER	RATING	UNIT
T <sub>STG</sub>	Temperature range	°C
P <sub>D</sub>	Storage	
	Power dissipation <sup>2</sup>	
	N package	mW
	F package	W
	I package	W
All input, output and supply voltages with respect to ground	-0.5 to 7	V

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## DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ <sup>3</sup>	Max	
$V_{IL}$ $V_{IH}$	Input voltage Low High	-0.5 2.2		0.65 $V_{CC}$	V
$V_{OL}$ $V_{OH}$	Output voltage Low High		$I_{OL} = 1.9\text{mA}$ $I_{OH} = -100\mu\text{A}$	2.2	0.45
$I_{LI}$	Input load current (All input pins)		$V_{IN} = 0$ to $5.25\text{V}$		$10\mu\text{A}$
$I_{LOH}$ $I_{LOL}$	Output leakage current		$\bar{CE} = 2.2\text{V}$ $V_{OUT} = 4.0\text{V}$ $V_{OUT} = 0.45\text{V}$		$10\mu\text{A}$ -100
$I_{CC1}$ $I_{CC2}$	Supply current	All inputs = $5.25\text{V}$ , Data out open $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$		30 40 40	mA

## AC ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$  unless otherwise specified,  
Input pulse levels =  $0.65\text{V}$  to  $2.2\text{V}$ , Input pulse rise and fall times =  $20\text{ns}$ ,  
Timing measurement reference level =  $1.5\text{V}$ , Output load = 1 TTL gate  
and  $C_L = 100\text{pF}$

PARAMETER	TO	FROM	21L02			21L02-1			21L02-2			21L02-3			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>READ CYCLE</b> $t_{RC}$ $t_A$ $t_{CO}$			1,000		500	1,000		500	650		400	400		ns	ns
$t_{OH1}$ $t_{OH2}$	Output time	Chip enable		50	0		50	0	50	0	50	0		ns	ns
<b>WRITE CYCLE</b> $t_{WC}$ $t_{WP}$ $T_{WR}$			1,000		500	750		400	650		400	250		ns	ns
$t_{AW}$ $t_{DW}$ $t_{DH}$ $t_{CW}$	Setup and hold time Setup time Hold time Setup time	Write Rise of R/W Change of data in Write	Address Data in Rise of R/W Chip enable	200 800 100 900		150 330 100 400		200 450 100 550		100 300 50 300				ns	

### NOTES

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated based on  $+150^\circ\text{C}$  maximum junction temperature and a thermal resistance of  $150^\circ\text{C/W}$  junction to ambient (B package).
- Typical values are at  $+25^\circ\text{C}$  and typical supply voltages.
- All inputs protected against static charge.
- Parameter valid over operating temperature range unless otherwise specified.
- All voltage measurements are referenced to ground.
- Manufacturer reserves the right to make design and process changes and improvements.

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## TIMING DIAGRAMS

