21L02-F,I,N • 21L02-1-F,I,N • 21L02-2-F,I,N • 21L02-3-F,I,N

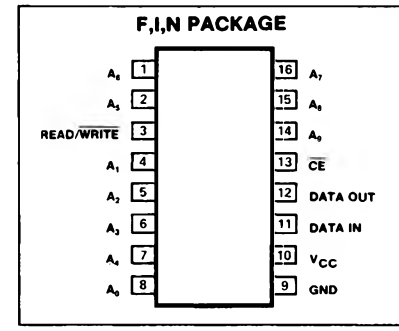
DESCRIPTION

The 21L02, 21L02-1, 21L02-2, and 21L02-3 are low power static random access read/write memories fabricated with low threshold n-channel silicon gate technology.

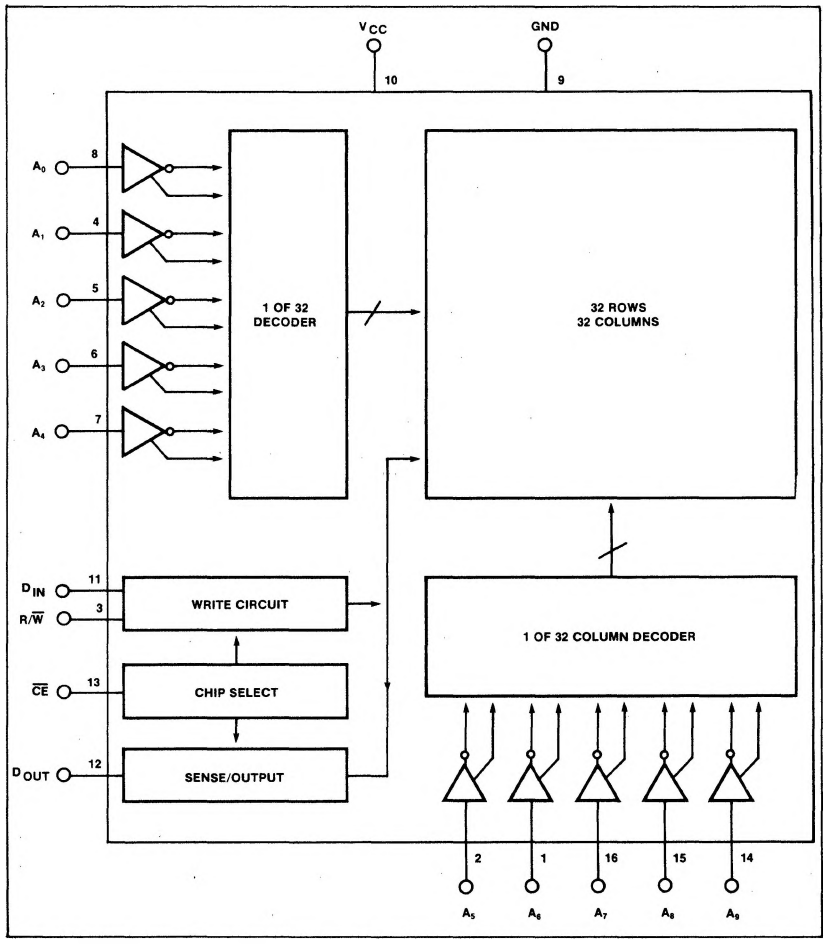
FEATURES

- **Fully static**
- **Requires no clocks**
- **Completely DTL/TTL compatible**
- **Single 5V power supply**
- **Three-state output for OR-tie capability**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation[2]		
	N package	640	mW
	F package	1	W
	I package	1	W
	All input, output and supply voltages with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.65	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.9mA			0.45	
V_{OH}	High	I_{OH} = -100μA	2.2			
I_{LI}	Input load current (All input pins)	V_{IN} = 0 to 5.25V			10	μA
	Output leakage current	$\overline{CE}$ = 2.2V				μA
I_{LOH}		V_{OUT} = 4.0V			10	
I_{LOL}		V_{OUT} = 0.45V			-100	
	Supply current	All inputs = 5.25V, Data out open				mA
I_{CC1}		T_A = 25°C		30	40	
I_{CC2}		T_A = 0°C			40	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified,
Input pulse levels = 0.65V to 2.2V, Input pulse rise and fall times = 20ns,
Timing measurement reference level = 1.5V, Output load = 1 TTL gate
and C_L = 100pF

PARAMETER		TO	FROM	21L02			21L02-1			21L02-2			21L02-3			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ CYCLE															
t_{RC}	Read cycle			1,000			500			650			400			ns
t_A	Access time					1,000			500			650		400		ns
t_{CO}		Output time	Chip enable			500			350			400		300		ns
	Previous read data valid with respect to															ns
t_{OH1}	Address			50			50			50			50			
t_{OH2}	Chip enable			0			0			0			0			
	WRITE CYCLE															
t_{WC}	Write cycle			1,000			500			650			400			ns
t_{WP}	Write pulse width			750			300			400			250			ns
T_{WR}	Write recovery time			50			50			50			50			ns
	Setup and hold time															ns
t_{AW}	Setup time	Write	Address	200			150			200			100			
t_{DW}	Setup time	Rise of R/$\overline{W}$	Data in	800			330			450			300			
t_{DH}	Hold time	Change of data in	Rise of R/$\overline{W}$	100			100			100			50			
t_{CW}	Setup time	Write	Chip enable	900			400			550			300			

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient (B package).
3. Typical values are at +25°C and typical supply voltages.
4. All inputs protected against static charge.
5. Parameter valid over operating temperature range unless otherwise specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.

TIMING DIAGRAMS