

## 1K I<sup>2</sup>C™ Serial EEPROM

### Device Selection Table

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
24AA01	1.8-5.5	400 kHz <sup>(1)</sup>	I
24LC01B	2.5-5.5	400 kHz	I, E

**Note 1:** 100 kHz for Vcc <2.5V

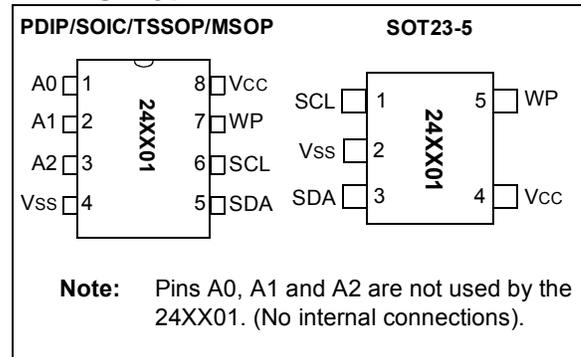
### Features

- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 1 µA standby current typical (I-temp)
- Organized as 1 block of 128 bytes (1 x 128 x 8)
- 2-wire serial interface bus, I<sup>2</sup>C™ compatible
- Schmitt trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (24AA01) and 400 kHz (24LC01B) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 erase/write cycles
- Data retention > 200 years
- 8-lead PDIP, SOIC, TSSOP, and MSOP package
- 5-lead SOT-23 package
- Available for extended temperature ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

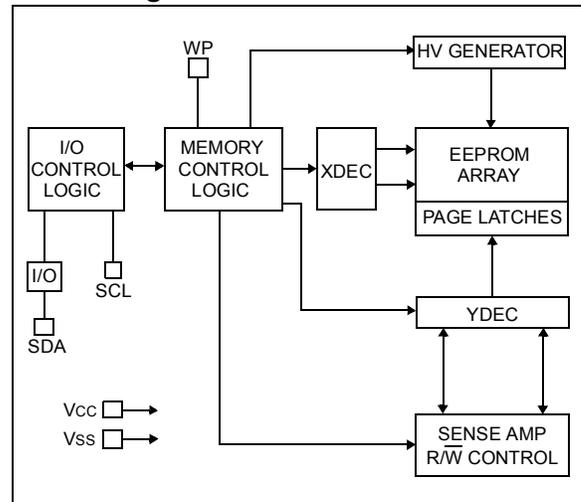
### Description

The Microchip Technology Inc. 24AA01/24LC01B (24XX01\*) is a 1 Kbit Electrically Erasable PROM. The device is organized as one block of 128 x 8-bit memory with a 2-wire serial interface. Low voltage design permits operation down to 1.8V with standby and active currents of only 1 µA and 1 mA respectively. The 24XX01 also has a page-write capability for up to 8 bytes of data. The 24XX01 is available in the standard 8-pin PDIP, surface mount SOIC, TSSOP and MSOP packages and is also available in the 5-lead SOT-23 package.

### Package Types



### Block Diagram



\*24XX01 is used in this document as a generic part number for the 24AA01/24LC01B devices.

# 24AA01/24LC01B

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

V <sub>CC</sub> .....	6.5V
All inputs and outputs w.r.t. V <sub>SS</sub> .....	-0.3V to V <sub>CC</sub> +1.0V
Storage temperature .....	-65°C to +150°C
Ambient temp. with power applied .....	-40°C to +125°C
ESD protection on all pins .....	≥ 4 kV

† **NOTICE:** Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### 1.1 DC Characteristics

DC CHARACTERISTICS			V <sub>CC</sub> = +1.8V to +5.5V Industrial (I): T <sub>AMB</sub> = -40°C to +85°C Automotive (E): T <sub>AMB</sub> = -40°C to +125°C				
Param. No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
D1	V <sub>IH</sub>	<b>WP, SCL and SDA pins</b>	—	—	—	—	—
D2	—	High level input voltage	0.7 V <sub>CC</sub>	—	—	V	—
D3	V <sub>IL</sub>	Low level input voltage	—	—	0.3 V <sub>CC</sub>	V	—
D4	V <sub>HYS</sub>	Hysteresis of Schmitt trigger inputs	0.05 V <sub>CC</sub>	—	—	V	<b>(Note)</b>
D5	V <sub>OL</sub>	Low level output voltage	—	—	0.40	V	I <sub>OL</sub> = 3.0 mA, V <sub>CC</sub> = 2.5V
D6	I <sub>LI</sub>	<b>Input leakage current</b>	—	—	±10	µA	V <sub>IN</sub> = .1V to V <sub>CC</sub>
D7	I <sub>LO</sub>	<b>Output leakage current</b>	—	—	±10	µA	V <sub>OUT</sub> = .1V to V <sub>CC</sub>
D8	C <sub>IN</sub> , C <sub>OUT</sub>	Pin capacitance (all inputs/outputs)	—	—	10	pF	V <sub>CC</sub> = 5.0V <b>(Note)</b> T <sub>AMB</sub> = 25°C, F <sub>CLK</sub> = 1 MHz
D9	I <sub>CC</sub> write	<b>Operating current</b>	—	0.1	3	mA	V <sub>CC</sub> = 5.5V, SCL = 400 kHz
D10	I <sub>CC</sub> read		—	0.05	1	mA	—
D11	I <sub>CCS</sub>	<b>Standby current</b>	—	0.01	1	µA	Industrial Automotive SDA = SCL = V <sub>CC</sub> WP = V <sub>SS</sub>
			—	—	5	µA	

**Note:** This parameter is periodically sampled and not 100% tested.

## 1.2 AC Characteristics

AC CHARACTERISTICS			VCC = +1.8V to +5.5V Industrial (I): TAMB = -40°C to +85°C Automotive (E): TAMB = -40°C to +125°C				
Param. No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
1	FCLK	Clock frequency	— —	— —	400 100	kHz	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA01)
2	THIGH	Clock high time	600 4000	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA01)
3	TLOW	Clock low time	1300 4700	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA01)
4	TR	SDA and SCL rise time (Note 1)	— —	— —	300 1000	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA01)
5	TF	SDA and SCL fall time	—	—	300	ns	(Note 1)
6	THD:STA	START condition hold time	600 4000	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA01)
7	TSU:STA	START condition setup time	600 4700	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA01)
8	THD:DAT	Data input hold time	0	— —	— —	ns	(Note 2)
9	TSU:DAT	Data input setup time	100 250	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA01)
10	TSU:STO	STOP condition setup time	600 4000	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA01)
11	TAA	Output valid from clock (Note 2)	— —	— —	900 3500	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA01)
12	TBUF	Bus free time: Time the bus must be free before a new transmission can start	1300 4700	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA01)
13	TOF	Output fall time from VIH minimum to VIL maximum	20+0.1CB —	— —	250 250	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA01)
14	TSP	Input filter spike suppression (SDA and SCL pins)	—	—	50	ns	(Notes 1 and 3)
15	TWC	Write cycle time (byte or page)	—	—	5	ms	—
16	—	Endurance	1M	—	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

**Note 1:** Not 100% tested. CB = total capacitance of one bus line in pF.

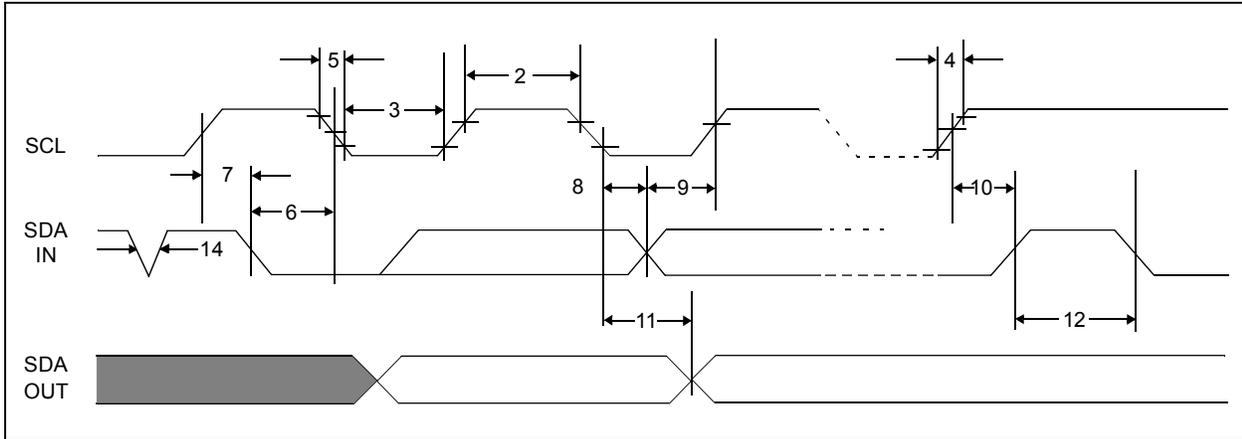
**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

**3:** The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a Ti specification for standard operation.

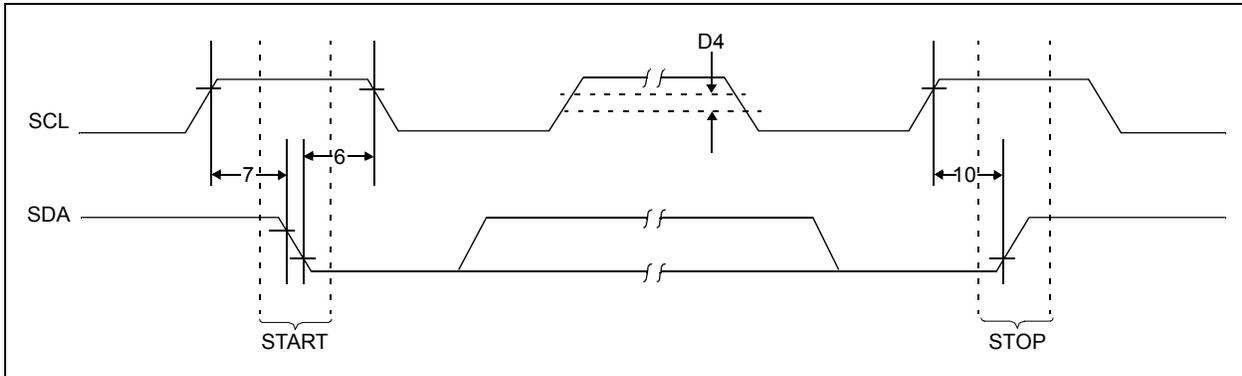
**4:** This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's website: [www.microchip.com](http://www.microchip.com).

# 24AA01/24LC01B

**FIGURE 1-1: BUS TIMING DATA**



**FIGURE 1-2: BUS TIMING START/STOP**



## 2.0 FUNCTIONAL DESCRIPTION

The 24XX01 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions, while the 24XX01 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

## 3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

### 3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

### 3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

### 3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

### 3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first-in first-out (FIFO) fashion.

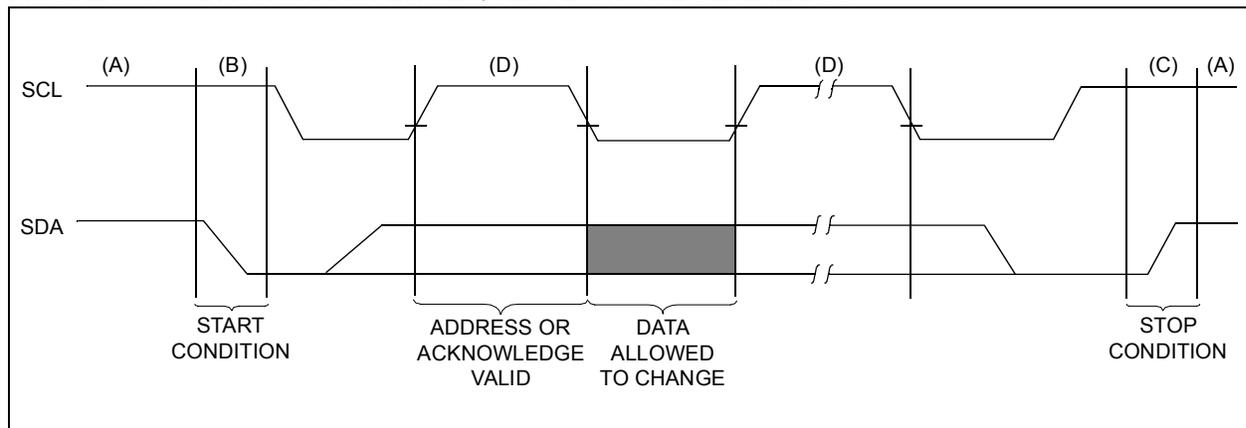
### 3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

**Note:** The 24XX01 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX01) will leave the data line HIGH to enable the master to generate the STOP condition.

**FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS**



# 24AA01/24LC01B

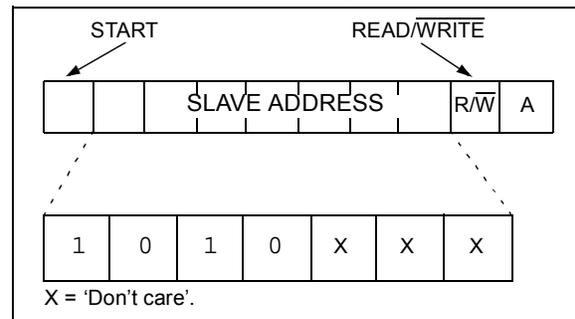
## 3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24XX01 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). The block select bits are 'don't care's' for the 24XX01.

The last bit of the control byte defines the operation to be performed. When set to '1' a read operation is selected, when set to '0' a write operation is selected. Following the START condition, the 24XX01 monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/W bit, the 24XX01 will select a read or write operation.

Operation	Control Code	Block Select	R/W
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



## 4.0 WRITE OPERATION

### 4.1 Byte Write

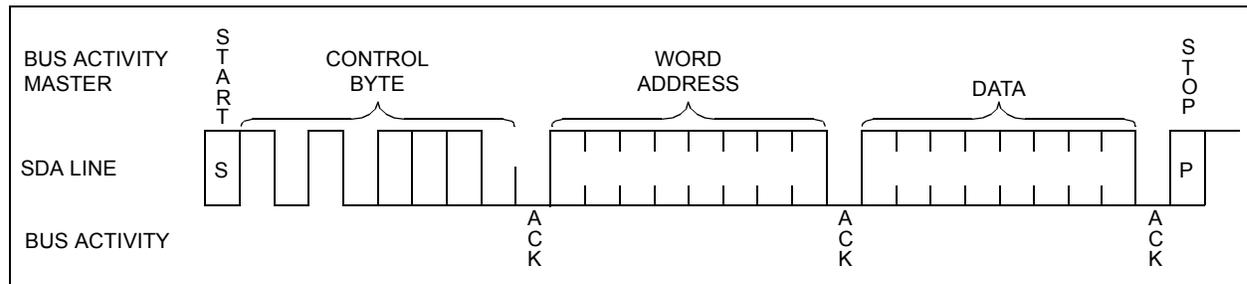
Following the START condition from the master, the device code (4 bits), the block address (3 bits, don't cares) and the R/W bit which is a logic LOW is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24XX01. After receiving another acknowledge signal from the 24XX01, the master device will transmit the data word to be written into the addressed memory location. The 24XX01 acknowledges again and the master generates a STOP condition. This initiates the internal write cycle, and during this time the 24XX01 will not generate acknowledge signals (Figure 4-1).

### 4.2 Page Write

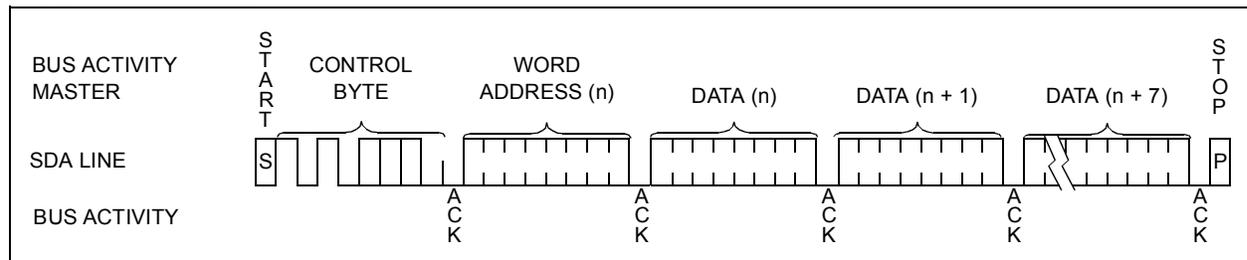
The write control byte, word address and the first data byte are transmitted to the 24XX01 in the same way as in a byte write. But instead of generating a STOP condition the master transmits up to 8 data bytes to the 24XX01, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a STOP condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by '1'. The higher order 7 bits of the word address remains constant. If the master should transmit more than 8 words prior to generating the STOP condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the STOP condition is received an internal write cycle will begin (Figure 4-2).

**Note:** Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

**FIGURE 4-1: BYTE WRITE**



**FIGURE 4-2: PAGE WRITE**



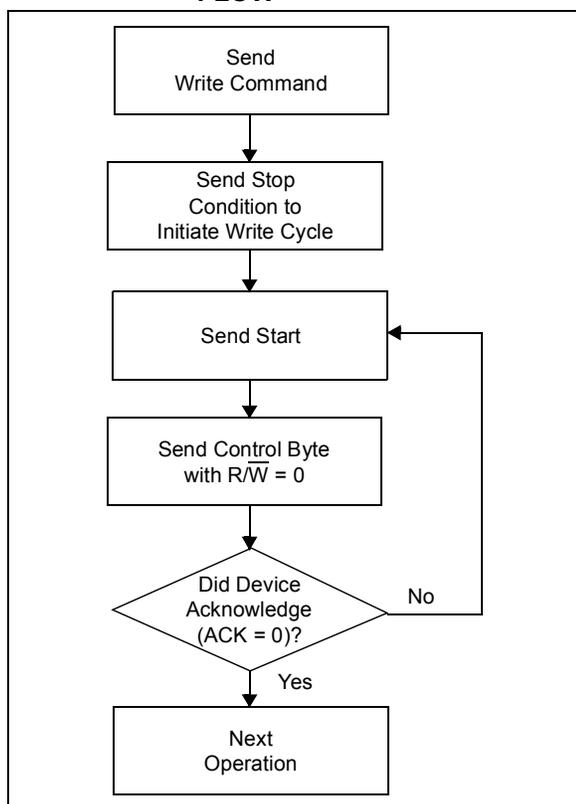
## 5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the STOP condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ( $R/\overline{W} = 0$ ). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

## 6.0 WRITE PROTECTION

The 24XX01 can be used as a serial ROM when the WP pin is connected to VCC. Programming will be inhibited and the entire memory will be write-protected.

**FIGURE 5-1: ACKNOWLEDGE POLLING FLOW**



## 7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the slave address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

### 7.1 Current Address Read

The 24XX01 contains an address counter that maintains the address of the last word accessed, internally incremented by '1'. Therefore, if the previous access (either a read or write operation) was to address  $n$ , the next current address read operation would access data from address  $n + 1$ . Upon receipt of the slave address with R/W bit set to '1', the 24XX01 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a STOP condition and the 24XX01 discontinues transmission (Figure 7-1).

### 7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24XX01 as part of a write operation. After the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/W bit set to a '1'. The 24XX01 will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a STOP condition and the 24XX01 discontinues transmission (Figure 7-2).

### 7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24XX01 transmits the first data byte, the master issues an acknowledge as opposed to a STOP condition in a random read. This directs the 24XX01 to transmit the next sequentially addressed 8-bit word (Figure 7-3).

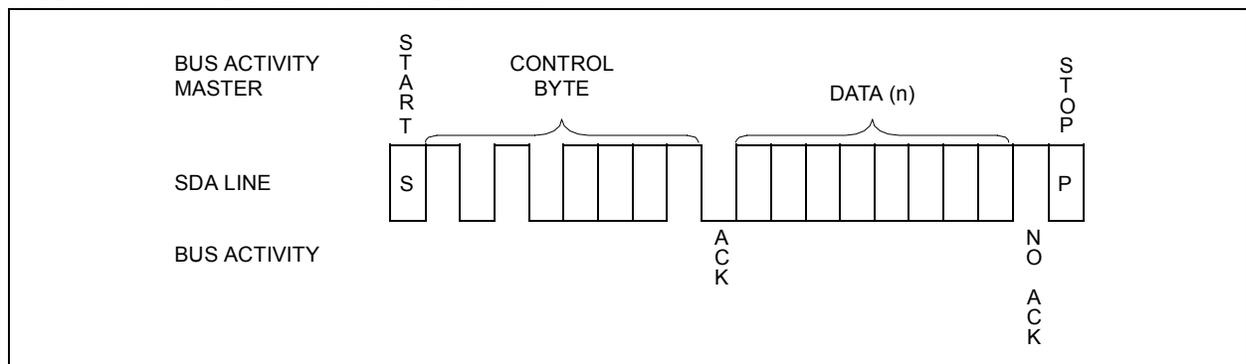
To provide sequential reads the 24XX01 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

### 7.4 Noise Protection

The 24XX01 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5V at nominal conditions.

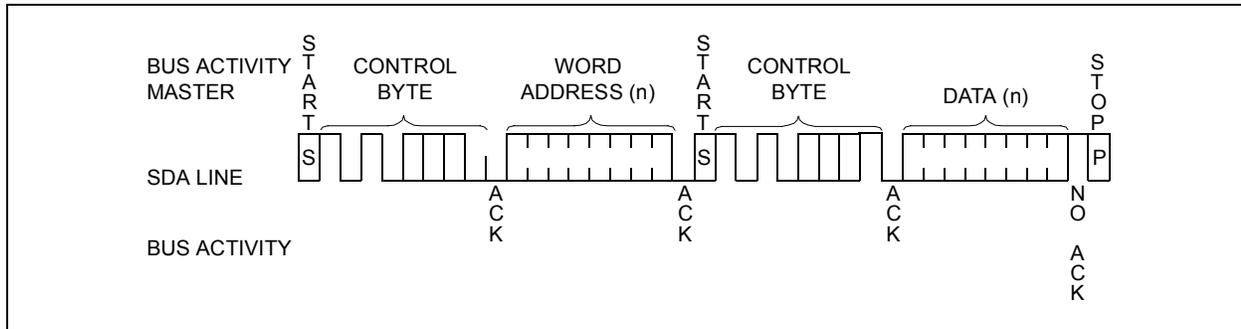
The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

**FIGURE 7-1: CURRENT ADDRESS READ**

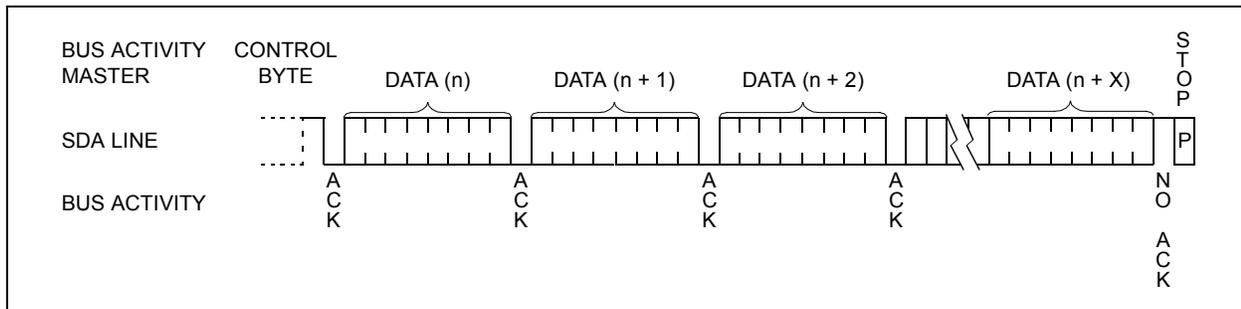


# 24AA01/24LC01B

**FIGURE 7-2: RANDOM READ**



**FIGURE 7-3: SEQUENTIAL READ**



## 8.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 8-1.

**TABLE 8-1: PIN FUNCTION TABLE**

Name	PDIP	SOIC	TSSOP	MSOP	SOT23	Description
A0	1	1	1	1	—	Not Connected
A1	2	2	2	2	—	Not Connected
A2	3	3	3	3	—	Not Connected
Vss	4	4	4	4	2	Ground
SDA	5	5	5	5	3	Serial Address/Data I/O
SCL	6	6	6	6	1	Serial Clock
WP	7	7	7	7	5	Write Protect Input
Vcc	8	8	8	8	4	+1.8V to 5.5V Power Supply

### 8.1 A0, A1, A2

These pins are not used by the 24XX01. They may be left floating or tied to either Vss or Vcc.

### 8.2 Serial Address/Data Input/Output (SDA)

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal. Therefore, the SDA bus requires a pull-up resistor to Vcc (typical 10 k $\Omega$  for 100 kHz, 2 k $\Omega$  for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

### 8.3 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

### 8.4 Write-Protect (WP)

This pin must be connected to either Vss or Vcc.

If tied to Vss normal memory operation is enabled (read/write the entire memory 00–7F).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

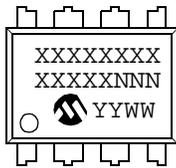
This feature allows the user to use the 24XX01 as a serial ROM when WP is enabled (tied to Vcc).

# 24AA01/24LC01B

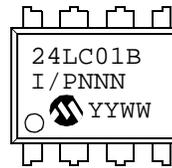
## 9.0 PACKAGING INFORMATION

### 9.1 Package Marking Information

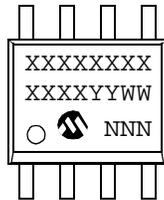
8-Lead PDIP (300 mil)



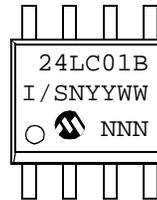
Example:



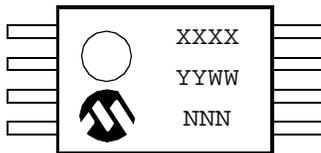
8-Lead SOIC (150 mil)



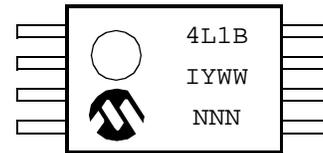
Example:



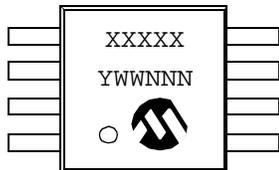
8-Lead TSSOP



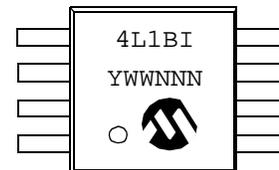
Example:



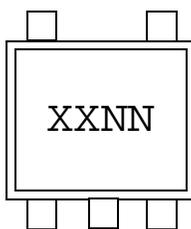
8-Lead MSOP



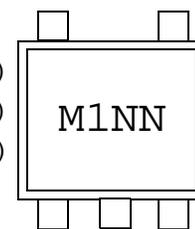
Example:



5-Lead SOT-23



Example:

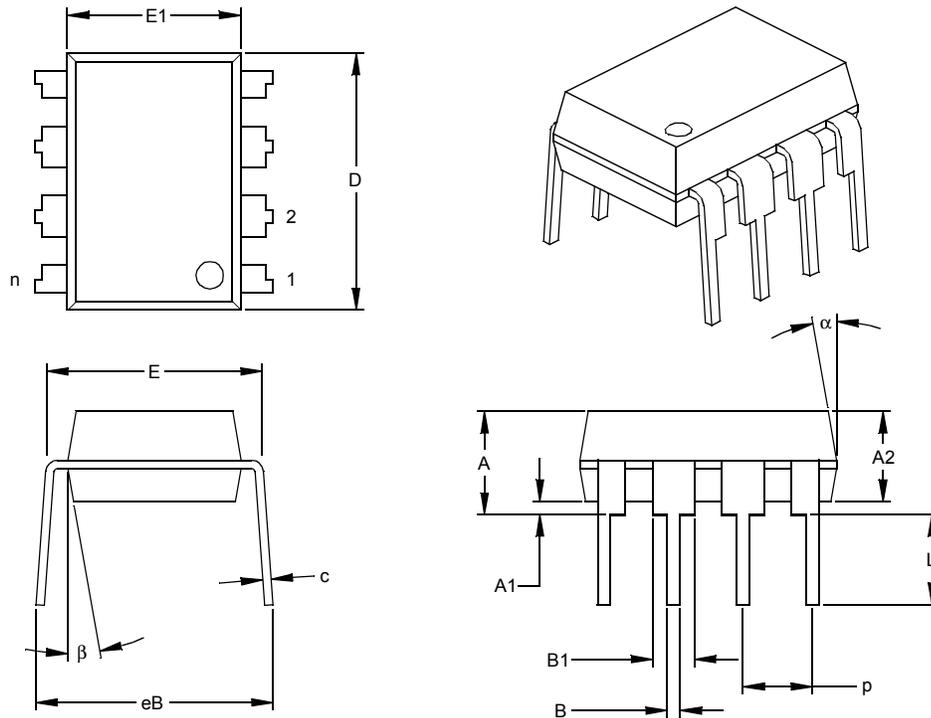


24AA01 = B1(I-Temp)  
 24LC01B = M1(I-Temp)  
 24LC01B = N1(E-Temp)

<b>Legend:</b>	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

\* Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

## 8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

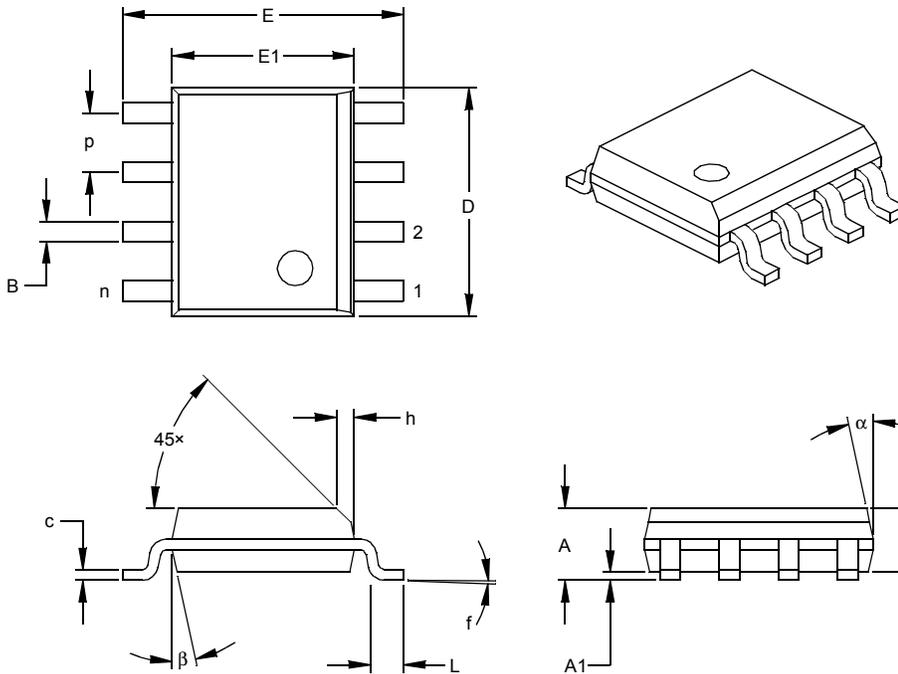
\* Controlling Parameter  
 § Significant Characteristic

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.  
 JEDEC Equivalent: MS-001  
 Drawing No. C04-018

# 24AA01/24LC01B

## 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	$\alpha$	0	12	15	0	12	15
Mold Draft Angle Bottom	$\beta$	0	12	15	0	12	15

\* Controlling Parameter  
 § Significant Characteristic

**Notes:**

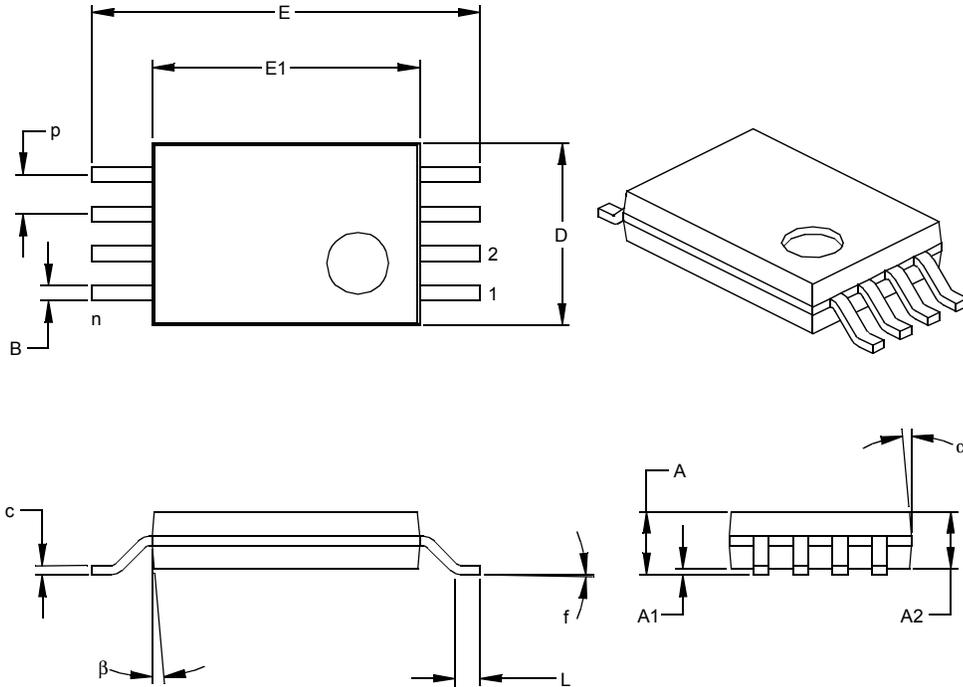
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

# 24AA01/24LC01B

## 8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter

§ Significant Characteristic

### Notes:

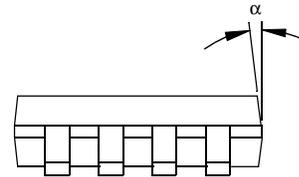
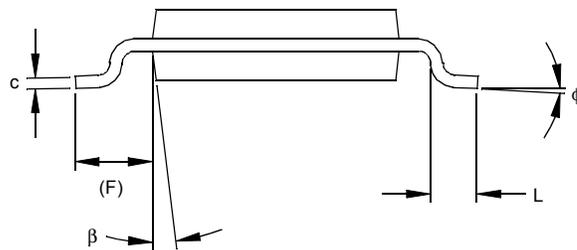
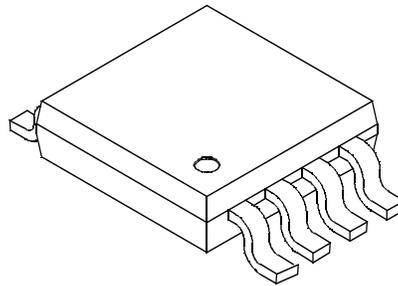
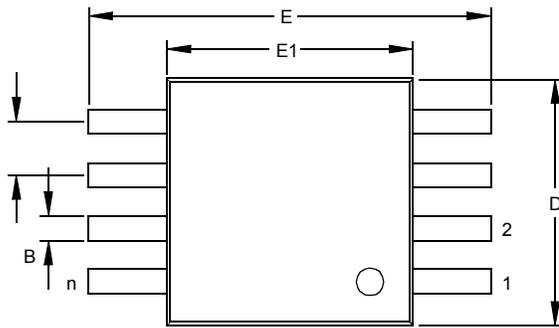
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JEDEC Equivalent: MO-153

Drawing No. C04-086

# 24AA01/24LC01B

## 8-Lead Plastic Micro Small Outline Package (MSOP)



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p	.026			0.65		
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

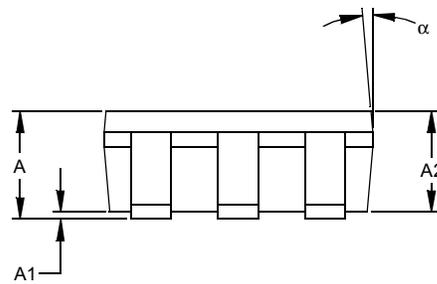
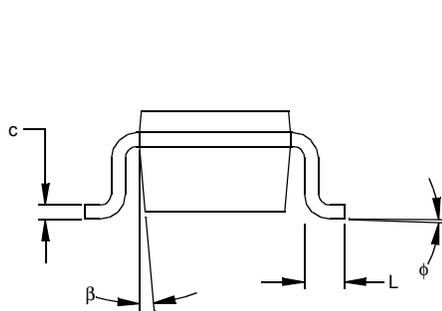
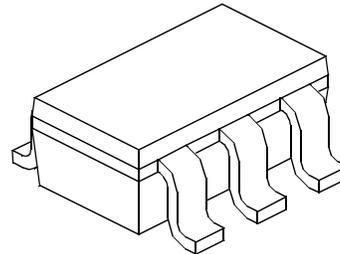
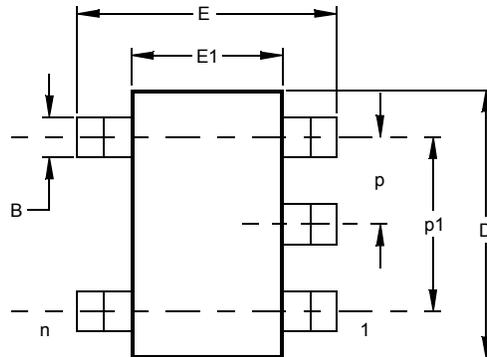
\*Controlling Parameter  
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-111

## 5-Lead Plastic Small Outline Transistor (OT) (SOT23)



Units		INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	$\phi$	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	$\alpha$	0	5	10	0	5	10
Mold Draft Angle Bottom	$\beta$	0	5	10	0	5	10

\* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-178

Drawing No. C04-091

# 24AA01/24LC01B

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Device	Temperature Range	Package	
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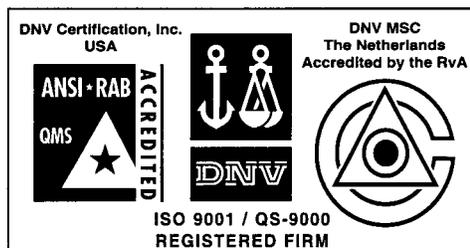
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