Signetics

FULLY DECODED, 256 X 1 STATIC RANDOM ACCESS MEMORY

2501

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2500 Series 256 x 1 Random Access Memory employs enhancement mode P-channel MOS devices integrated on a single monolithic chip. It is fully decoded, permitting the use of a 16-pin dual in-line package. Complete static operation requires no clocking.

FEATURES

- FULLY DECODED ADDRESS
- ACCESS TIME – 1.0μs GUARANTEED
- POWER DISSIPATION -1.6mW/BIT MAXIMUM DURING ACCESS
- STANDBY POWER DISSIPATION – 50 μW/BIT
- DTL AND TTL COMPATIBLE
- CHIP SELECT AND OUTPUT WIRED-OR CAPABILITY FOR EASY EXPANSION
- STANDARD 16-PIN DIP SILICONE PACKAGE
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY
- V_{CC} = +5V, V_{DD} = V_D = -9V

APPLICATIONS

SMALL BUFFER STORES
SMALL CORE MEMORY REPLACEMENT
BIPOLAR COMPATIBLE DATA STORAGE

SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

PROCESS TECHNOLOGY

The use of Signetics' unique Silicon Gate Low Threshold Process allows the design and production of higher performance MOS circuits and provides higher functional density on a chip than other MOS technologies.

BIPOLAR COMPATIBILITY

All inputs of the 2501 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 2.0 mA, sufficient to drive one standard TTL load.

POWER DISSIPATION

The maximum power dissipation of 1.6mW/bit is required only during Read or Write. For standby operation, 50μW/bit is obtained by removing V_D and reducing V_{DD} to −2.0V. Removal of V_D alone will cut power dissipation by a factor of 1.5.

SPECIAL FEATURE

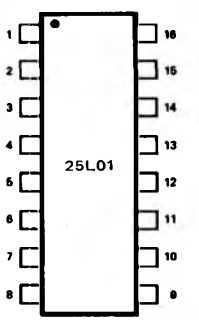
The outputs of the 2501 are effectively open circuited when the device is not selected (logic 1 on chip select). This feature allows OR-Tying for memory expansion.

PART IDENTIFICATION TABLE

TYPE	PACKAGE	OP. TEMP. RANGE
2501B	16-pin Silicone DIP	0°C. to +70°C.
2501I	16-pin Ceramic DIP	0°C. to +70 C.

PIN CONFIGURATION (Top View)

B/I PACKAGE



1. Address 6
2. Address 8
3. Address 7
4. V_D
5. V_{CC}
6. Address 5
7. Address 1
8. V_{DD}
16. $\overline{\text{Chip Select}}$
15. R/W
14. $\overline{\text{Data Out}}$
13. Data Out
12. Data In
11. Address 4
10. Address 2
9. Address 3

MAXIMUM GUARANTEED RATINGS (1)

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{CC}	+0.3V to -20V
Supply Voltages V_{DD} and V_D with Respect to V_{CC}	-18V
Power Dissipation at T_A = 70°C	640mW

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{ILI}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

NOTE: Special devices are available for operation at V_{DD} = -7V, V_D = -10V. Contact your Signetics Representative for details.

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V (8), V_{DD} = V_D = -9V ±5%, unless otherwise specified. See notes below)

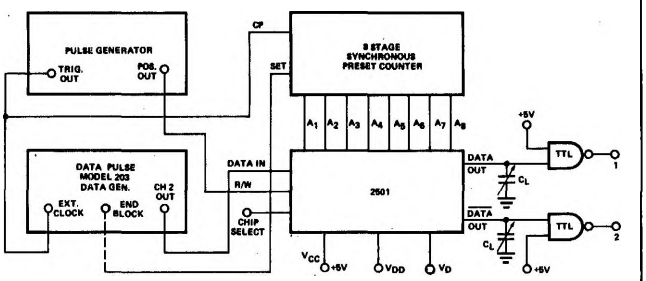
SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)		<1.0	500	nA	V_{IN} = 0.0V; T_A = +25°C
I_{LO}	Output Leakage Current		<1.0	1000	nA	V_{OUT} = 0.0V, Chip Select Input = +3.3V, T_A = +25°C
I_{DD}	Power Supply Current, V_{DD}		13.0	18	mA	T_A = +25°C, V_{DD} = V_D = −9V
I_D	Power Supply Current, V_D		8.5	12	mA	I_{OL} = 0.0mA T_A = +25°C V_{DD} = V_D = −9V
V_{IL}	Input "Low" Voltage	−12		V_{CC}−4.5	V	
V_{IH}	Input "High" Voltage	V_{CC}−2.0		V_{CC}+0.3	V	
I_{OL1}	Output Sink Current	3.0	6		mA	V_{OUT} = +0.45V, T_A = +25°C
I_{OL2}	Output Sink Current	2.0	5		mA	V_{OUT} = +0.45V, T_A = +70°C
I_{OL3}	Output Sink Current		6	13	mA	V_{OUT} = −0.7 V
I_{OH1}	Output Source Current	−3.0	4		mA	V_{OUT} = 0.0V, T_A = +25°C
I_{OH2}	Output Source Current	−2.0	3		mA	V_{OUT} = 0.0V, T_A = +70°C
V_{OL}	Output "Low" Voltage		−0.7	+0.45	V	I_{OL} = 3.0 mA
V_{OH}	Output "High" Voltage	+3.5	+4.5		V	I_{OH} = −100μA
C_{IN}	Input Capacitance (All Input Pins)		7	10	pF	V_{IN} = +5.0V f = 1 MHz
C_{OUT}	Output Capacitance		7	10	pF	V_{OUT} = +5.0 V f = 1 MHz

SWITCHING CHARACTERISTICS

Guaranteed Limits $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V$ (8), $V_{DD} = V_D = -9V \pm 5\%$ except as noted.

READ CYCLE			WRITE CYCLE		
SYMBOL	TEST	LIMITS (μsec) MAX	SYMBOL	TEST	LIMITS (μsec) MIN.
t_a	Access Time	1.0μsec	t_{WD}	Address to Write Pulse Delay	0.3
			t_{WP}	Write Pulse Width	0.4
			t_W	Write Time	0.3
			t_{DO}	Data-Write Pulse Overlap	0.1

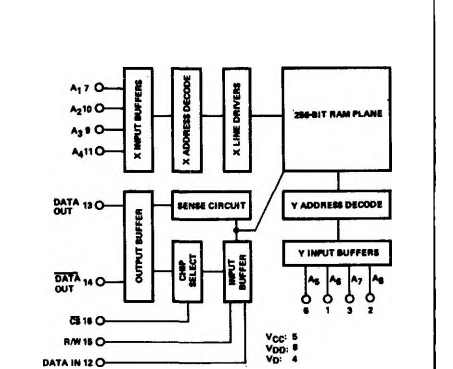
TEST SETUP FOR SPEED MEASUREMENT



NOTES:

1. Each clock time is split into a Read followed by a Write. Read and Write times can be varied by adjustment of the "delay" and "width" controls of the pulse generator.
2. Data generator produces a 256-bit block of data, 32 bits repeated 8 times, "PCM" mode used so data can be changed in 32 bits of the 2501 from one cycle to the next.
3. All inputs to the 2501 are standard TTL outputs with V_{CC} = +5V ±5%.
4. Access time is measured between A1 (least significant address input) and points 1 and 2.

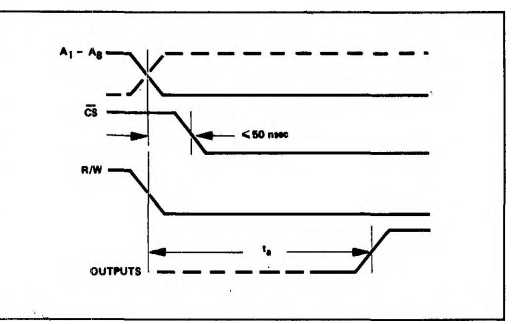
BLOCK DIAGRAM



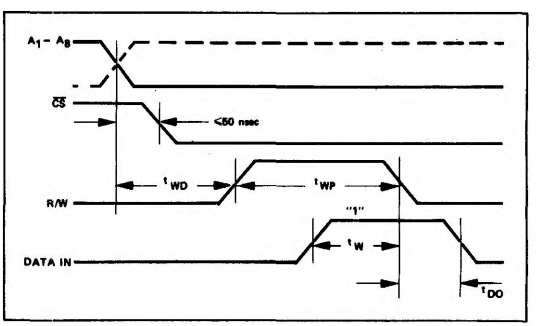
CONDITIONS OF TEST

Input pulse amplitudes: 0 to +5V, Input pulse rise and fall times: < 10 nsec. Speed measurements referenced to 1.5V levels. Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{pd} \leq 10$ nsec)

READ CYCLE (For Measurement Purpose Only)

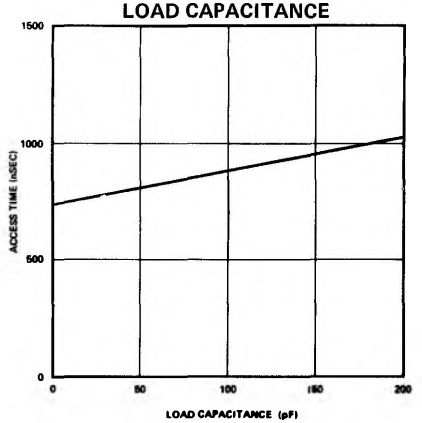


WRITE CYCLE (For Measurement Purpose Only)

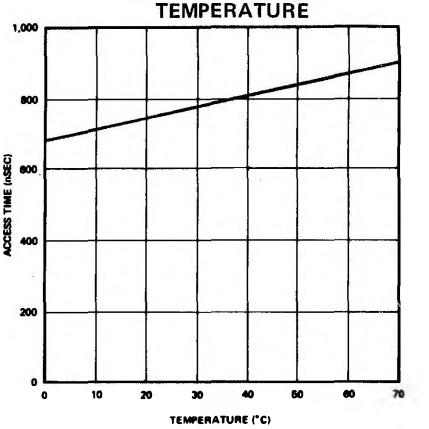


TYPICAL CHARACTERISTICS [1]

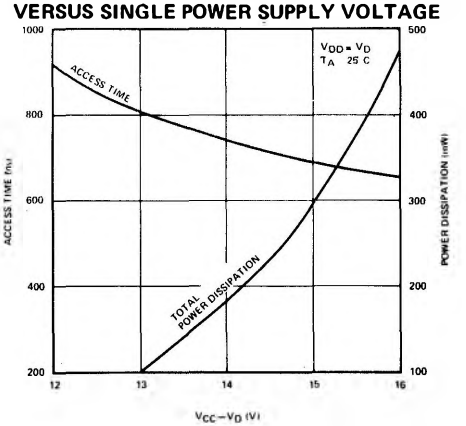
ACCESS TIME VERSUS LOAD CAPACITANCE



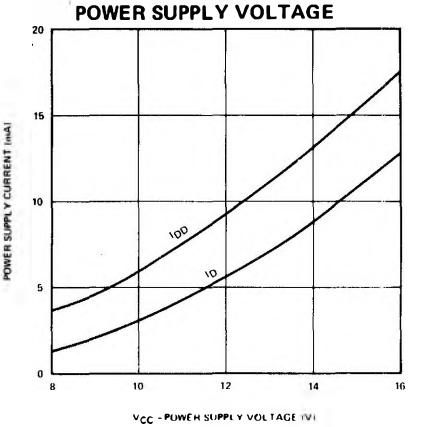
ACCESS TIME VERSUS TEMPERATURE



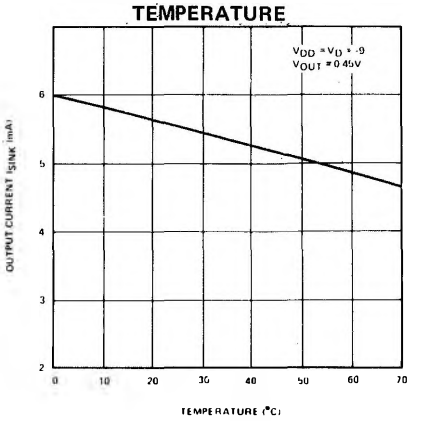
TYPICAL ACCESS TIME AND POWER DISSIPATION VERSUS SINGLE POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT VERSUS POWER SUPPLY VOLTAGE



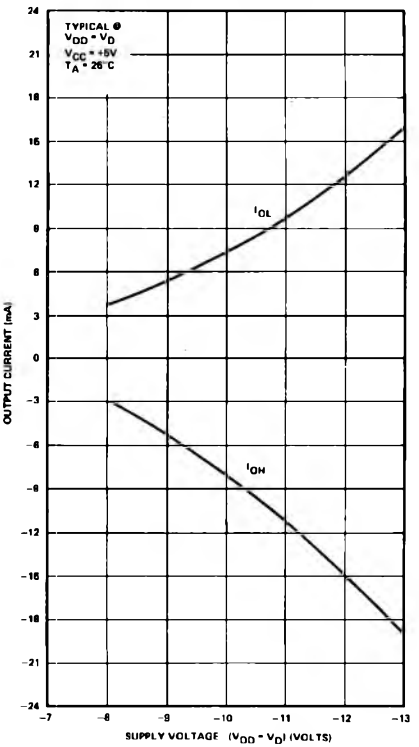
OUTPUT CURRENT VERSUS TEMPERATURE



(1) NOTE: For all typical curves, V_{CC} = 5V, $V_{DD} = V_D$ = -9V, T_A = 25°C (unless otherwise noted).

TYPICAL CHARACTERISTICS (Cont'd)

OUTPUT CURRENT VERSUS SUPPLY VOLTAGE



APPLICATION INFORMATION

OPERATION

The 2501 is a 256 x 1 Random Access Memory element. It is fully decoded and provides control for Read/Write and Chip Select modes. The operation of this element is described below.

ADDRESSING

An 8-bit address code will select any one of 256 bits for either Read or Write operation. All address input logic levels are compatible with standard bipolar TTL or DTL logic levels.

READ

A logic "0" level (∿0V) applied to the R/W control will result in a Read operation. This can be presented to the R/W control simultaneously or before application of an address code. In this mode the information from the memory will be available on the outputs less than 1μsec later than the application of an address code. Note that there is no need to re-write the data into the memory after a read operation since the read is non-destructive.

WRITE

A "Write" command is a logic "1" (≥+3.3V) level to the R/W control. This should be presented to the chip no sooner than 300 nsec after the application of an address code. This time delay is necessary for proper address decoding. This "Write" command has to be present for at least 400 nsec to insure that the information is written into the memory. The "Write" command should be off (i.e., memory should be in "Read" mode) by the time the address code is changed. The input data should be present for at least the last 300 nsec of the "Write" command.

CHIP SELECT

The memory array is inhibited with the application of a logic "1" (≥+3.3V) to the Chip Select control. This will render both R/W and Data Input leads ineffective and will stop information transfer through the output buffer. The address decoder, however, will not be inhibited. This feature allows an effective increase in memory speed. (See below) The output leads are open while the memory array is inhibited. This allows OR-Tying of many memory arrays.

RANDOM ACCESS MEMORY

Arbitrary size memories can be built by tying appropriate numbers of 2501's together. Figure 1 shows a block diagram of a memory system containing 256 N words by M bits. For example, if the memory size were 4096 words by 12 bits, N = 16 and M = 12. Thus the number of 2501's required is M x N = 192. The address inputs A_1 through A_8 are common to all the rows. Inputs C_1 through C_n provide the column select and are wired to the Chip Select inputs of the 2501's. For the example of the 4096 word memory, a 12-bit address must be specified. The first 8 bits would drive inputs A_1 through A_8 directly. The remaining 4 bits would have to be decoded externally into the 16 lines required for the 16 columns. A block diagram of the 4096 x 12 memory is shown in Figure 2. Any number of 2501's can be OR-tied together, however, access time is affected by capacitive loading (approximately 1 nsec/pF). Each 2501 output represents 7 pF (typical) of loading, but the amount of stray capacitance contributed by the printed circuit board wiring can vary greatly and must be determined for each application. Figure 3 shows two different bit line organizations where the capacitive load that must be driven by the 2501 is reduced by employing logic gates to perform the OR-ing function. The organization of Figure 3b results in the minimum load capacitance but requires more gates per bit line than other organizations.

SEQUENTIAL MEMORY

On applications such as program memory or table lookup, where memory operations are highly sequential, but non-synchronous, the memory may be organized for a faster

SEQUENTIAL MEMORY (Cont'd).

average memory cycle than in the true random access case. This involves using the fact that access may be made through the chip select input in 0.2 μsec (typically) where a typical access time if one of the address inputs (A_1-A_8) changes, is 0.8 μsec. For the case of the 4096 word memory organized in this fashion information can be read out at an average access time of 0.25 μsec since access is made through the Chip Select input 15/16 of the time.

LOW POWER OPERATION

Another feature of this memory element is its capability of operating at very low standby power levels. The only time the element has to dissipate full power (~1.6mW/bit) is when it is exercised by either "Write" or "Read" operation. In the standby mode, when the chip will only store information, but does not need to be accessed, the peripheral power supply (V_D) is completely shut off. This will immediately cut the total power drain by a factor of 1.5.

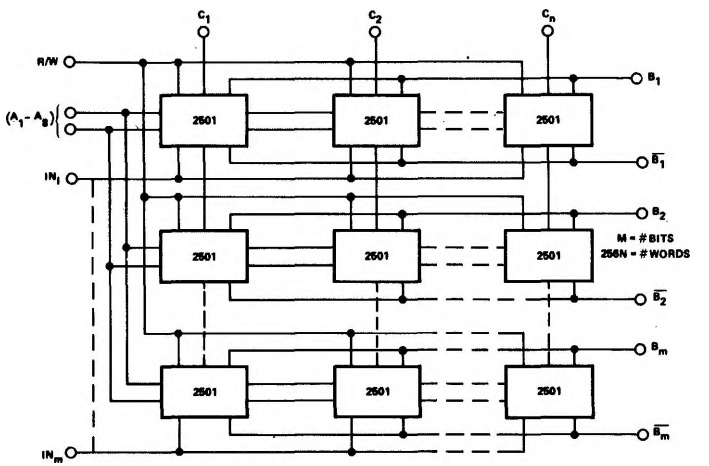


FIGURE 1. ORGANIZATION OF 2501's INTO LARGER MEMORY

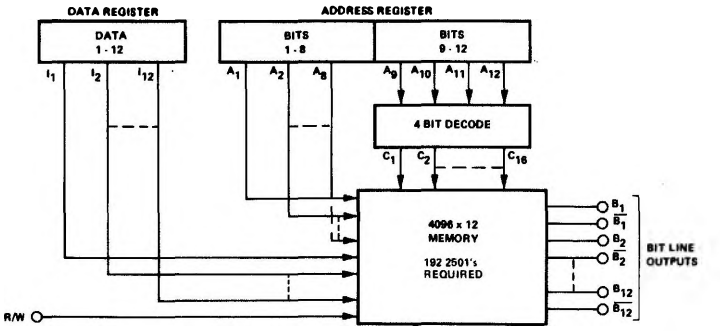
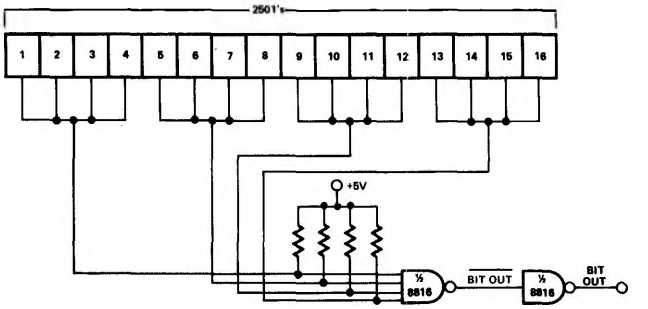
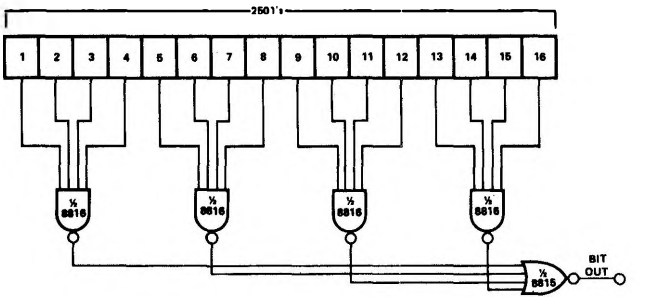


FIGURE 2. ORGANIZATION OF 4096 WORD BY 12-BIT MEMORY



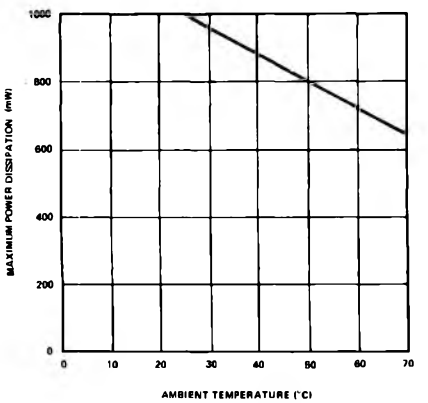
a. Combination of wire-ORing and logic-ORing of 2501's



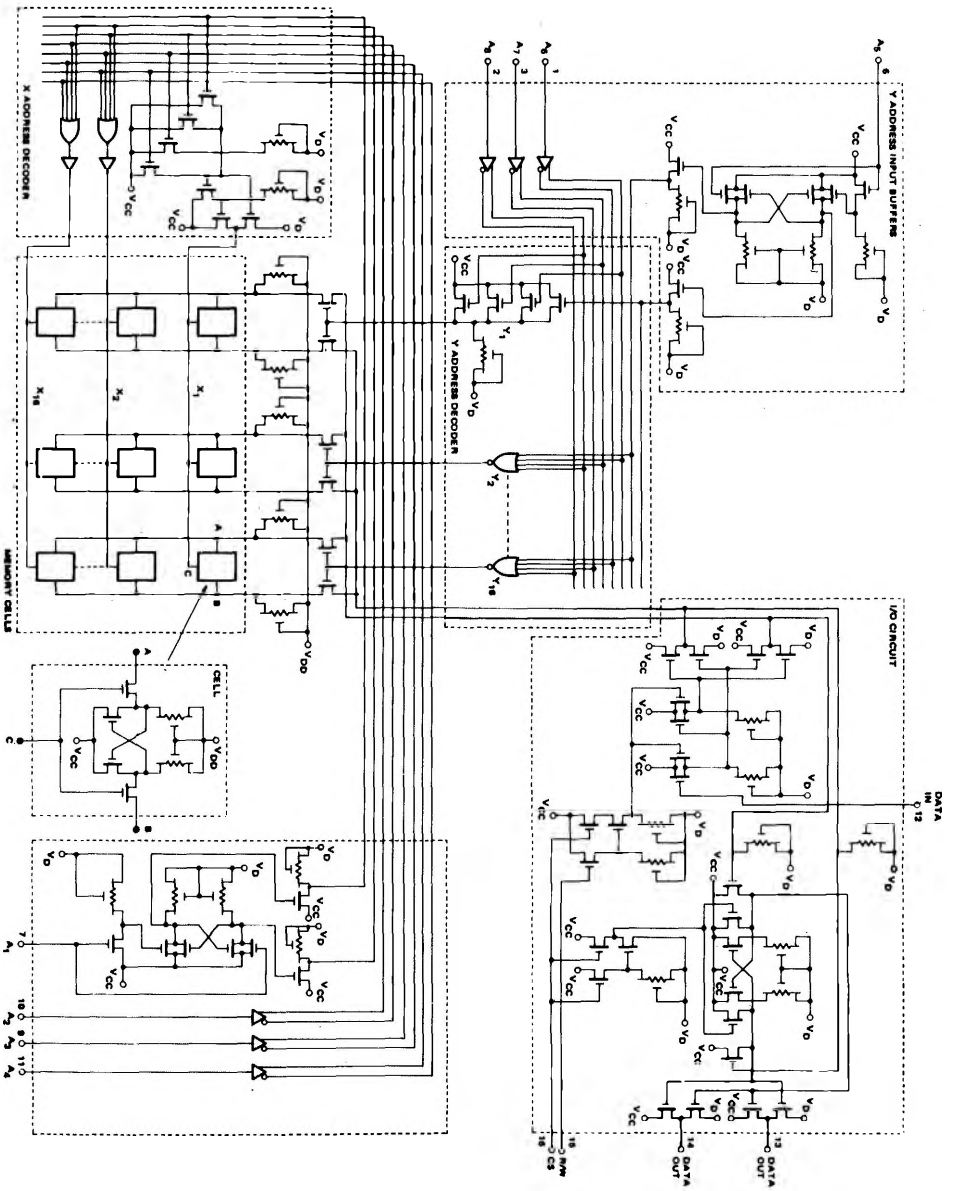
b. Logic-ORing of 2501's

FIGURE 3. BIT LINE ORGANIZATIONS TO MINIMIZE CAPACITIVE LOAD–4096 WORDS

PACKAGE MAXIMUM POWER DISSIPATION



CIRCUIT SCHEMATIC



Signetics 2501 256 X 1 Static Random Access Memory