1024-BIT MULTIPLEXED DYNAMIC SHIFT REGISTER (256X4) 2502
1024-BIT MULTIPLEXED DYNAMIC SHIFT REGISTER (512X2) 2503
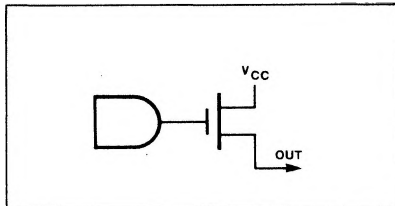## 1024-BIT MULTIPLEXED DYNAMIC SHIFT REGISTER (1024X1) 2504
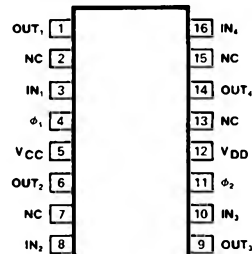
2502-N • 2503-TA,N • 2504-TA,N

DESCRIPTION

These 2500 Series 1024-bit multiplexed dynamic shift registers consist of enhancement mode p-channel MOS devices integrated on a single monolithic chip. Due to on-chip multiplexing, the data rate is twice the clock rate.
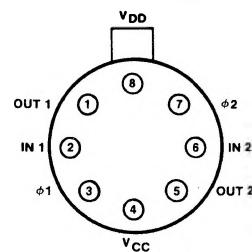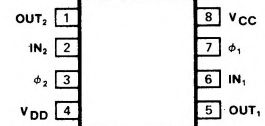
OUTPUT BUFFER

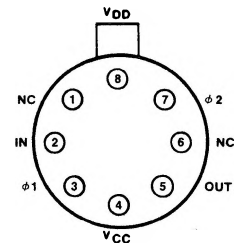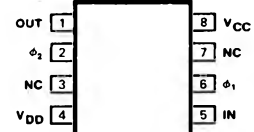## PIN CONFIGURATIONS

2502 N PACKAGE

OUT₁	1	16	IN₄
NC	2	15	NC
IN₁	3	14	OUT₄
φ₁	4	13	NC
V_CC	5	12	V_DD
OUT₂	6	11	φ₂
NC	7	10	IN₃
IN₂	8	9	OUT₃

2503 TA PACKAGE

2503 N PACKAGE

OUT₂	1	8	V_CC
IN₂	2	7	φ₁
φ₂	3	6	IN₁
V_DD	4	5	OUT₁

2504 TA PACKAGE

2504 N PACKAGE

OUT	1	8	V_CC
φ₂	2	7	NC
NC	3	6	φ₁
V_DD	4	5	IN

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range[2]		°C
T_A	Operating	0 to 70	
T_STG	Storage	–65 to 150	
P_D	Power dissipation T_A = 70° C[2]		mW
	TA and N (8-pin) package	535	
	N (16-pin) package	640	
	Data and clock input voltages and supply voltages with respect to V_CC[3]	0.3 to –20	V

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1024-BIT MULTIPLEXED DYNAMIC SHIFT REGISTER (1024X1)   2504

2502-N • 2503-TA,N • 2504-TA,N

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{DD} = -5V \pm 5\%$, $V_{CC} = 5V$[4] unless otherwise specified[5,6,7,8]

PARAMETER		TEST CONDITIONS	Min	Typ	Max	UNIT
	Input voltage					V
V_{IL}	Low				1.05	
V_{IH}	High		3.2		5.3	
V_{ILC}	Clock low		-10		-12	
V_{IHC}	Clock high		4.0		5.3	
	Output voltage					V
V_{OL}	Low	$R_L = 3K$, depends on R_L and TTL gate		-0.3		
V_{OH1}	High, driving MOS	$R_L = 5.6K$	3.6	4.0		
V_{OH2}	High, driving TTL	$R_L = 3K$	3.0	3.5		
I_{LI}	Input load current	$V_{IN} = V_{CC}$ to V_{DD}, $T_A = 25°C$			500	nA
	Leakage current	$T_A = 25°C$				nA
I_{LO}	Output	$V_{\phi 1} = V_{\phi 2} = -10V$, $V_{OUT} = 0.0V$		10	1000	
I_{LC}	Clock	$V_{ILC} = -10V$		10	1000	
I_{DD}	Supply current	Outputs at logic low, 4MHz data rate, $\phi 1 = \phi 2 = 85ns$ continuous operation, $V_{ILC} = -12V$, $T_A = 25°C$		15	25	mA
	Capacitance	At 1MHz, 25mV p-p, $T_A = 25°C$				pF
C_{IN}	Input		2.5		5	
C_{OUT}	Output		2.5		5	
C_ϕ	Clock		110		150	

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{DD} = -5V \pm 5\%$, $V_{CC} = 5V$[3], $V_{ILC} = -11V$[4,5,6,7]

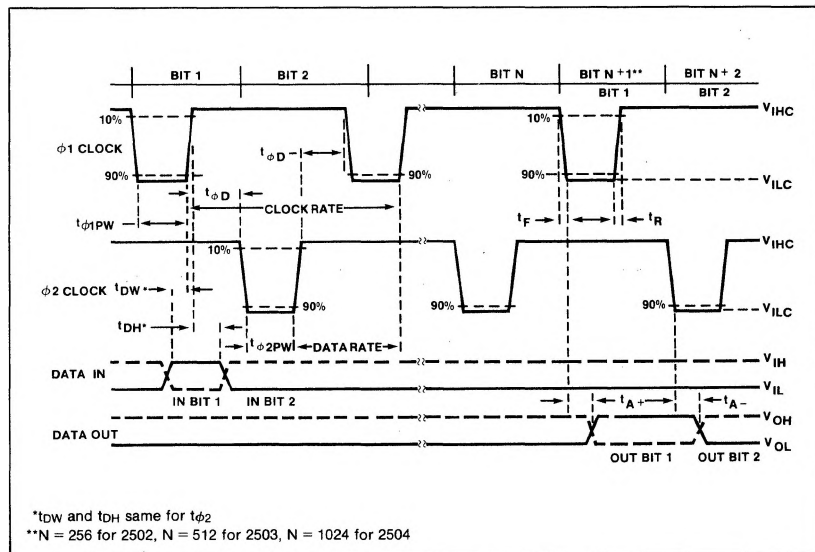| PARAMETER		Min	Typ	Max	UNIT
Freq.	Rep rate				MHz
	Clock	0.0005		4	
	Data	0.001		8	
ϕ_{PW}	Clock pulse width	85			ns
ϕ_D	Clock pulse delay	10			ns
t_R, t_F	Clock pulse transition	10		1000	ns
t_W	Data write time (setup)	50			ns
t_{DO}	Data in overlap	10			ns
t_{A+}, t_{A-}	Data out			90	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W (TA and V package) or 125°C/W (B package).
3. All inputs are protected against static charge.
4. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
5. Parameters are valid over operating temperature range unless specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserving the right to make design and process changes and improvements.
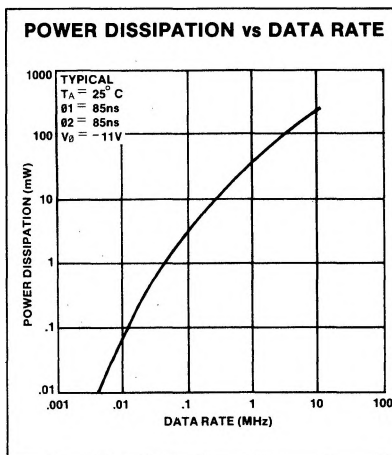8. Typical values are at +25°C and typical supply voltages.

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TIMING DIAGRAM

*t_{DW} and t_{DH} same for $t_{\phi2}$
**N = 256 for 2502, N = 512 for 2503, N = 1024 for 2504

TYPICAL PERFORMANCE CHARACTERISTICS

POWER DISSIPATION vs DATA RATE

TYPICAL APPLICATIONS

DTL/TTL/MOS INTERFACES

When interfacing MOS to MOS output resistors should be 4.7K min.

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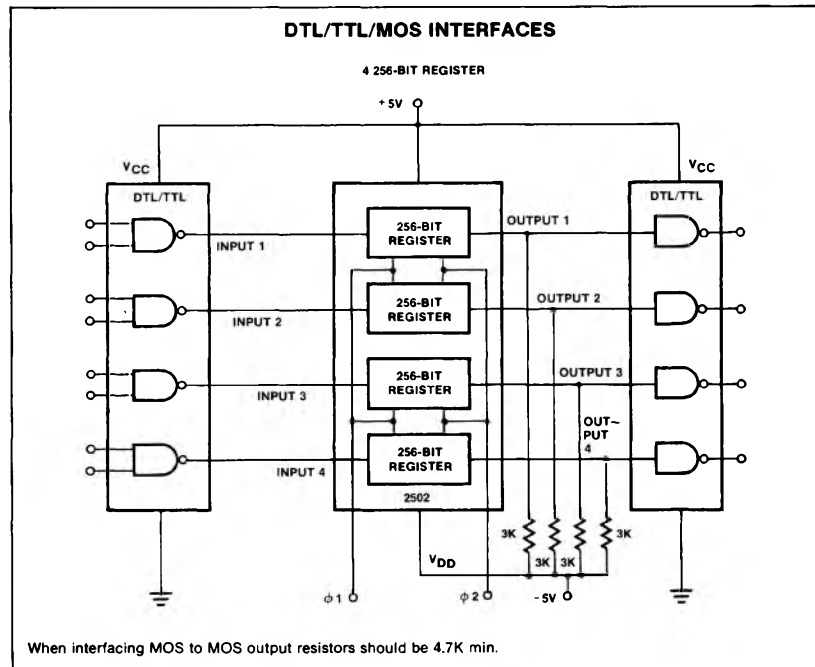
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TYPICAL APPLICATIONS (Cont'd)

WRITE/RECIRCULATE LOGIC

All resistors 3kΩ 5%