Signetics HIGH SPEED 64 X 7 X 5 CHARACTER GENERATOR | 2513

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2513 is a high speed 2560-bit Static ROM available in 64x7x5, and 64x8x5 versions. The product uses +5V, -5V and -12V power supplies, 5V TTL level input signals and Tri-State-Outputs for directs, low cost interfacing with TTL, DTL and 2500 Series MOS.

FEATURES

- 450 ns TYPICAL ACCESS TIME
- STATIC OPERATION
- TTL/DTL COMPATIBLE INPUTS
- +5, -5, -12V POWER SUPPLIES
- TRI-STATE OUTPUT CONTROLLED BY CHIP ENABLE FOR POWERFUL BUSSING CAPABILITY
- 2513/CM2140 ASCII FONT STANDARD (7 X 5)
- 24-PIN DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

RASTER SCAN CRT DISPLAYS (ROW OUTPUT)
PRINTER CHARACTER GENERATOR
PANEL DISPLAYS AND BILLBOARDS
MICRO-PROGRAMMING
CODE CONVERSION

PROCESS TECHNOLOGY

The use of Signetics' unique Silicon Gate Low Threshold Process allows the design and production of higher functional density and operating speed than other techniques.

SILICONE PACKAGING

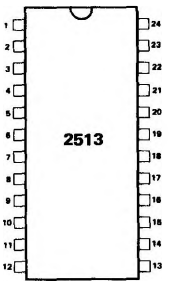
Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, superior moisture resistance, and ionic contamination barriers. For further information reference Signetics - "Silicone Package Qualification Report".

BIPOLAR COMPATIBILITY

All inputs of the 2513 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc). The data output buffers are capable of sinking a minimum of 1.6 mA, sufficient to drive one standard TTL load.

PIN CONFIGURATION (Top View)

N/I PACKAGE



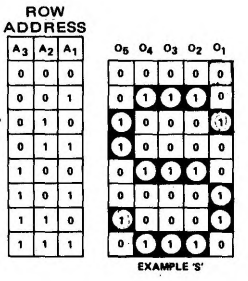
1.	V_{GG}	24.	V_{CC}
2.	NC	23.	NC
3.	NC	22.	Address 9
4.	Out 1	21.	Address 8
5.	Out 2	20.	Address 7
6.	Out 3	19.	Address 6
7.	Out 4	18.	Address 5
8.	Out 5	17.	Address 4
9.	NC	16.	Address 3
10.	Ground	15.	Address 2
11.	Chip Enable	14.	Address 1
12.	V_{DD}	13.	NC

PART IDENTIFICATION TABLE

PART	ORGANIZATION	PROGRAMMING
2513N/I CM2140	64X8X5	ASCII Font
2513N/I CMXXXX	64X7X5 64X8X5	Custom*

*Ask for "Signetics 2513/2514 Read Only Memory Software Package"

CHARACTER FORMAT



CHARACTER ADDRESS

	A4	A5	A6	A7	A8	A9
ASCII CHARACTER	1	1	0	0	1	0

MAXIMUM GUARANTEED RATINGS(1)

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation(2) @T_A 70°C	730mW
Input(3) and Supply Voltages with respect to V_{CC}	+0.3 to -20V

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}. V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V (8) ; V_{DD} =-5V; V_{GG} = -12V ±5% unless otherwise noted. (Notes 4, 5, 6, 7)

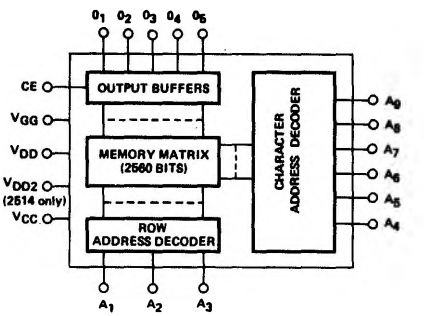
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = -5.5V T_A = 25°C V_{CE} = V_{CC}
I_{DD}	V_{DD} Power Supply Current		12	15	mA	Outputs Open
I_{GG}	V_{GG} Power Supply Current		10	15	mA	Outputs Open V_{CE} = V_{CC}
V_{IL}	Input Logic "0"			1.05	V	
V_{IH}	Input Logic "1"	3.2		5.3	V	

AC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5V (8); V_{DD} =-5V ±5%; V_{GG} = -12V ±5%; unless otherwise noted.

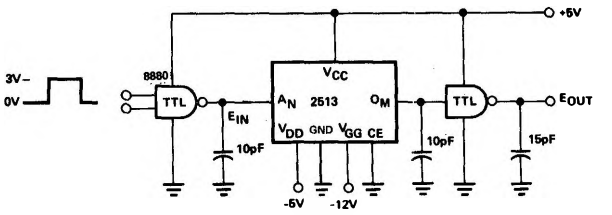
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "Zero"	-5		0.4	V	One TTL Load
V_{OH}	Output Logic "One"	3.0			V	One TTL Load
$^tCA_{(CM2140)}$	Character Access Time		500	600	ns	See AC Test Setup
^tRA	Row Access Time (A_1 - A_3)		450	500	ns	See AC Test Setup
^tCE	Chip Enable to Output		150		ns	
C_{IN}	Address Input Capacitance			10	pF	f = 1 MHz, V_{IH} = V_{CC}, 25mV p - p

BLOCK DIAGRAM

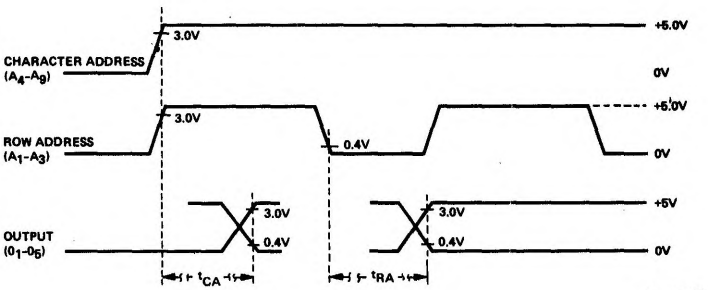


CE	OUTPUT
0	DATA
1	OPEN

AC TEST SETUP



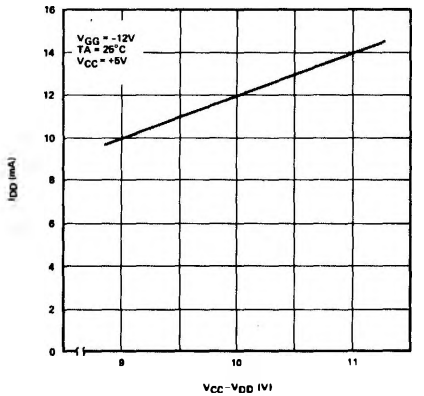
TIMING DIAGRAM (ADDRESS TIME)



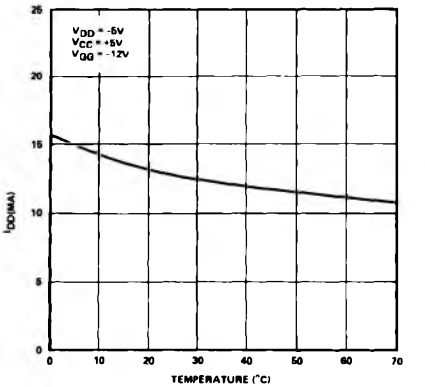
t_{CA} = Character Access Time
t_{RA} = Row Access Time

CHARACTERISTIC CURVES

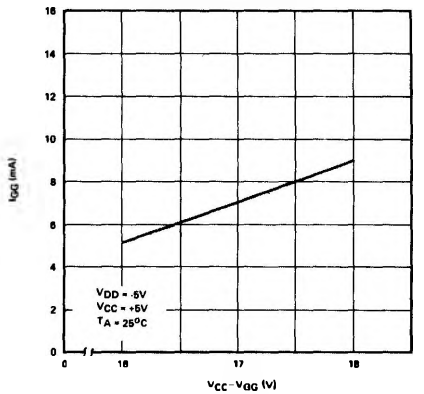
V_{DD} POWER SUPPLY CURRENT VERSUS VOLTAGE



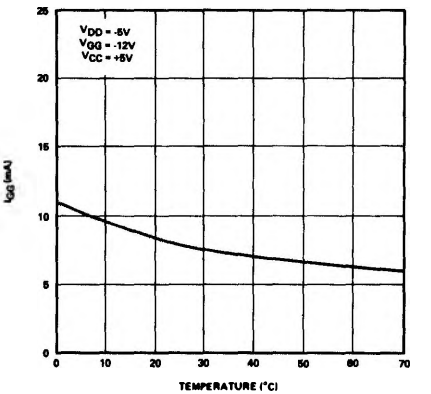
V_{DD} POWER SUPPLY CURRENT VERSUS TEMPERATURE



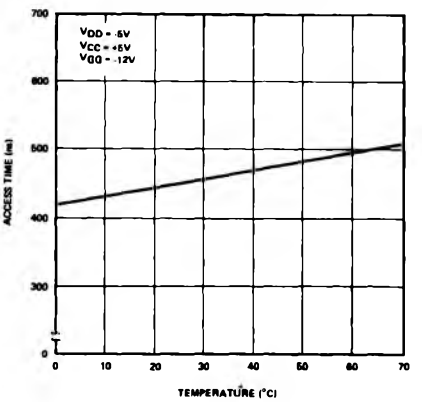
V_{GG} POWER SUPPLY CURRENT VERSUS VOLTAGE



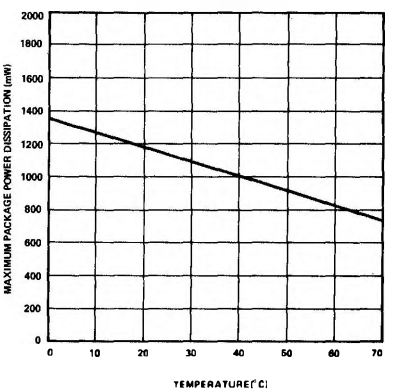
V_{GG} POWER SUPPLY CURRENT VERSUS TEMPERATURE



TYPICAL ACCESS TIME VERSUS TEMPERATURE

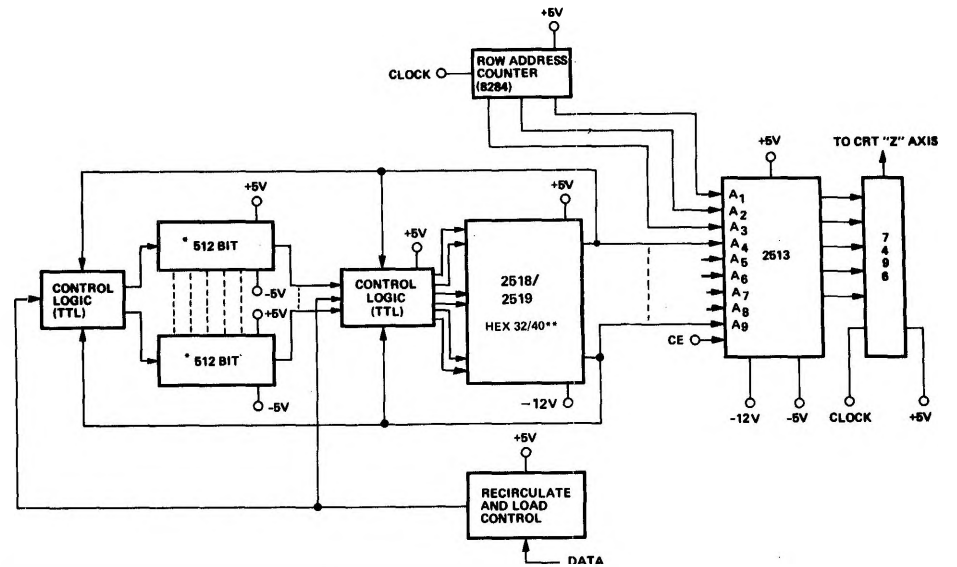


MAXIMUM PACKAGE POWER DISSIPATION



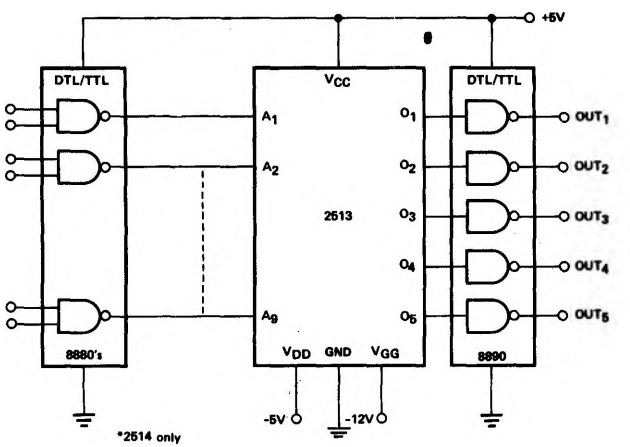
APPLICATIONS INFORMATION

CRT DISPLAY MEMORY AND CHARACTER GENERATOR



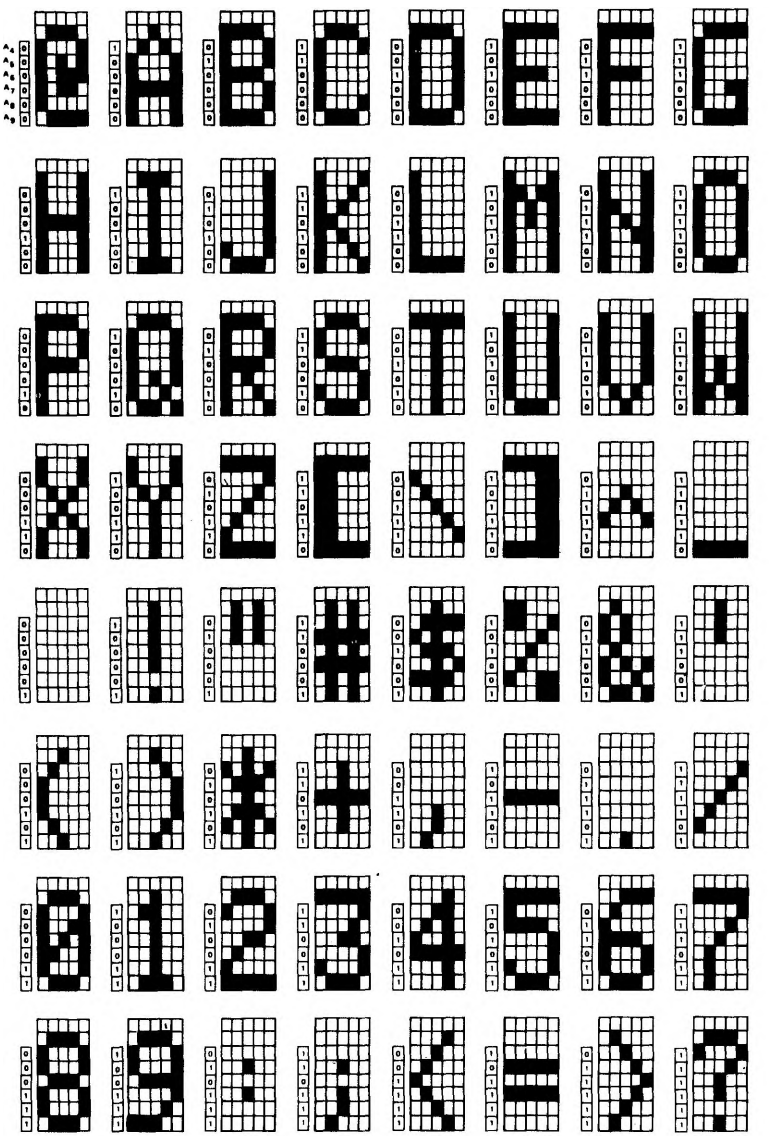
NOTE: *512 or 1024 Bit Shift Registers (2503, 2504, 2505, 2512)
** or Hex 64 BIT Two 2518's
Hex 72 BIT 2518 + 2519's

DTL/TTL INTERFACING



ASCII CHARACTER FONT

2513NX/CM2140



CIRCUIT SCHEMATIC