

DESCRIPTION

These Signetics 2500 Series dual 100-bit Dynamic Shift Registers consist of enhancement mode p-channel MOS devices integrated on a single monolithic chip. They use 2 clock phases.

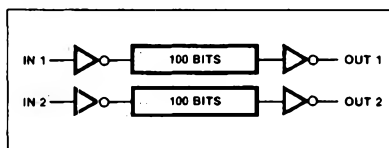
FEATURES

- 2506: Bare drain
- 2507: 7.5K Pull down
- 2517: 20K Pull down

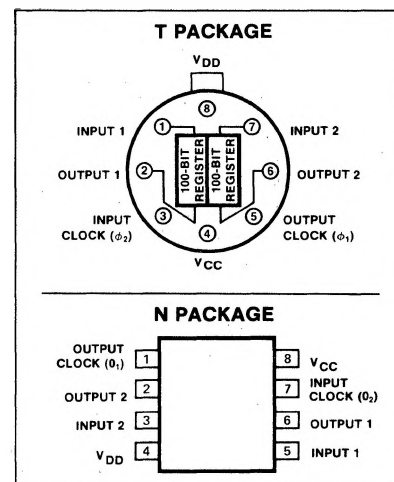
ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING	UNIT
T_A Temperature range		°C
Operating	0 to 70	
T_{STG} Storage	-65 to 150	
P_D Power dissipation at $T_A = 70^\circ\text{C}^2$		mW
T package	535	
N package	455	
Clock input voltages with respect to V_{CC}^3	0.3 to -20	V
Supply and data input voltages with respect to V_{CC}^3	0.3 to -12	V

BLOCK DIAGRAM



PIN CONFIGURATIONS



DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = -5V \pm 5\%$, $V_{CC} = 5V^4$, unless otherwise specified.^{5,6,7,8}

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{IL} Input voltage ⁹ Low		-5		1.05	V
V_{IH} Input voltage ⁹ High		3.2		5.3	V
V_{ILC} Clock low		-12		-10	V
V_{IHC} Clock high		4		5.3	V
V_{OH1} Output voltage ⁹ High (driving MOS)	$R_{INT} = 7.5k$ typ, $C_L = 10pF$, 2507 only $R_{INT} = 20k$ typ, 2517 only	3.4	4.0		V
V_{OH2} Output voltage ⁹ High (driving TTL)	$R_L = 3.3k$, $V_{DD} = -5V$, 2506 only	3.0	3.5		V
I_{LI} Load current Input 1	$T_A = 25^\circ\text{C}$ OUT 1, ϕ_1 , ϕ_2 and $V_{CC} = 5V$, IN 2, OUT 2 and IN 1 = -5.5V, $V_{DD} = -4.5V$		10	500	nA
Input 2	OUT 2, ϕ_1 , ϕ_2 and $V_{CC} = 5V$, IN 1, OUT 1 and IN 2 = -5.5V, $V_{DD} = -4.5V$		10	500	nA
I_{LO} Leakage current ¹⁰ Out 1	$T_A = 25^\circ\text{C}$ IN 1, V_{CC} , OUT 2 and $\phi_2 = 5V$, IN 2, V_{DD} and OUT 1 = -5.5V, $\phi_1 = -5V$		10	1000	nA
Out 2	IN 1, OUT 1, V_{CC} and $\phi_2 = 5V$, IN 2, V_{DD} and OUT 2 = -5.5V, $\phi_1 = -5V$		10	1000	nA
I_{LC} Clock leakage current ϕ_1 ϕ_2	$T_A = 25^\circ\text{C}$, $V_{DD} = -4.5V$, All other pins 5V $V_{\phi 1} = -12V$ $V_{\phi 2} = -12V$		10 10	1000 1000	nA
I_{DD} V_{DD} supply current	Outputs at logic low or high 3MHz, $\phi_1 = 150ns$, $\phi_2 = 100ns$		12	26	mA
C_{IN} Capacitance Input (1 and 2)	1MHz, 25mV p-p $V_{IN} = V_{CC}$		2.5	5	pF
C_ϕ Clock input (ϕ_1, ϕ_2)	$V_\phi = V_{CC}$		25	40	pF

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{DD} = -5V \pm 5\%$, $V_{CC} = 5V^4$, $V_{ILC} = -11V$

PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Freq. Clock rep rate				.0006	4	3	MHz
$\phi 1PW$ Pulse width $\phi 2PW$ Clock $\phi 1$ Clock $\phi 2$			At 3MHz	150 100			ns
ϕd Clock pulse delay			At 3MHz	10			ns
t_R, t_F Clock pulse transition			At 3MHz	10			ns
t_W Setup time	$\phi 2$	Data in		75		1000	ns
t_{DO} Data in overlap			$t_{R02} = t_{R01} = 10\text{ns}$	10			ns
t_{A+} Delay time	Data out	$\phi 1$	$V_\phi = V_{CC} - 16V$, Data out = 2.5V		90	150	ns

NOTES

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated based on a $+150^\circ\text{C}$ maximum junction temperature and a thermal resistance of 150°C/W (T package) or 175°C/W (V package).
- All inputs are protected against static charge.
- V_{CC} tolerance is $\pm 5\%$. Any variation in actual V_{CC} will be tracked directly by V_{IL} , V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
- Parameters are valid over operating temperature range unless otherwise specified.
- All voltage measurements are referenced to ground.
- Manufacturer reserves the right to make design and process changes and improvements.
- Typical values are at $+25^\circ\text{C}$ and typical supply voltages.
- Logic Convention: Data Lines - Positive; Clocks - Negative.
- V_{OL} (for this bare drain device) is a function only of the driven gate characteristics together with the external pull-down resistor. (R_{PD}).

TIMING DIAGRAM