signetics

HEX 32-HEX 40-BIT STATIC SHIFT REGISTERS

2518
2519

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series Hex 32 and 40-bit recirculating static shift registers consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals are provided for maximum interfacing capability.

FEATURES

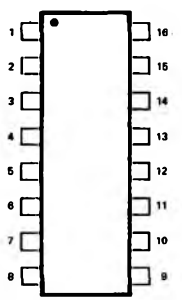
- TYPICAL CLOCK AND DATA RATE = 3MHz
- TTL/DTL COMPATIBLE CLOCK (SINGLE) PROVIDES EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- TWO BIT LENGTHS AVAILABLE
- SINGLE-ENDED (BARE DRAIN) BUFFERS
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGE – 16 PIN DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
LINE PRINTERS
CARD EQUIPMENT BUFFERS

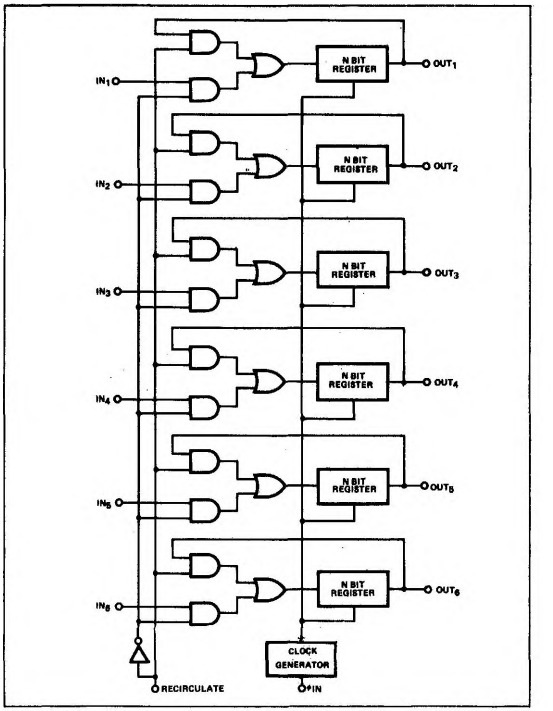
PIN CONFIGURATION (Top View)

B/I PACKAGE



1. IN_4	16. V_{CC}
2. IN_5	15. IN_3
3. IN_6	14. IN_2
4. Recirculate	13. IN_1
5. V_{GG}	12. OUT_1
6. Clock	11. OUT_2
7. OUT_6	10. OUT_3
8. OUT_5	9. OUT_4

BLOCK DIAGRAM



TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
1	0	Recirculate
1	1	Recirculate
0	0	"0" is Written
0	1	"1" is Written

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2518B	HEX 32	16-Pin Silicone DIP
2518I	HEX 32	16-Pin Ceramic DIP
2519B	HEX 40	16-Pin Silicone DIP
2519I	HEX 40	16-Pin Ceramic DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation at T_A = 70°C	640 mW
Data and Clock Input Voltages and Supply Voltages with Respect to V_{CC}	+0.3V to -20V

NOTES:

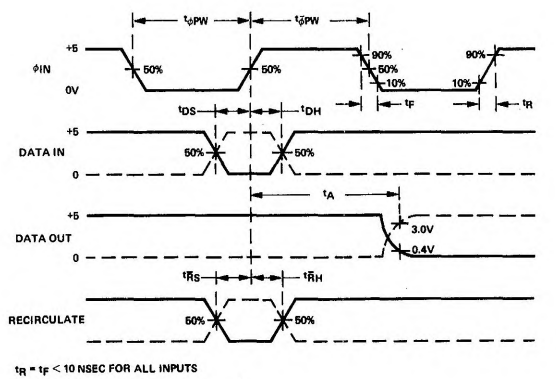
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 125°C C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5% Any variation in actual V_{CC} will be tracked directly by V_{IL}. V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
9. V_{OL} is dependent on R_L and characteristics of driven gate.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V (8); V_{GG} = -12V ± 5% unless otherwise noted. (Notes: 3,4,5,6,7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	500	nA	V_{in} =-5.5V, T_A = 25°C
I_{LO}	OUTPUT LEAKAGE CURRENT		10	1000	nA	T_A = 25°C
I_{LC}	CLOCK LEAKAGE CURRENT		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{GG}	POWER SUPPLY CURRENT		16	25	mA	CONTINUOUS OPERATION T_A = 25°C F = 2MHz
V_{IL}	INPUT "LOW" VOLTAGE			1.05	V	
V_{IH}	INPUT "HIGH"VOLTAGE	3.2		5.3	V	
V_{ILC}	CLOCK INPUT "LOW" VOLTAGE			1.05	V	
V_{IHC}	CLOCK INPUT "HIGH" VOLTAGE	3.2		5.3	V	

TIMING DIAGRAM

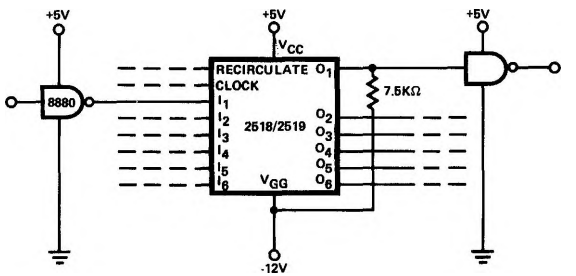


$t_R = t_F < 10$ NSEC FOR ALL INPUTS

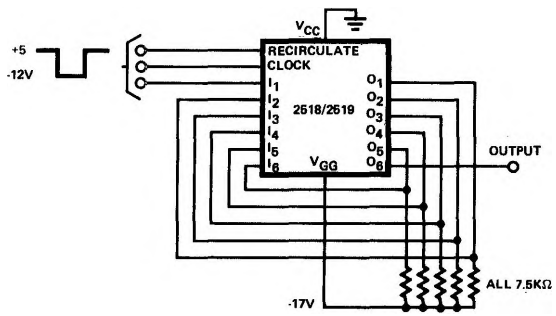
Note: Input rise and fall times: 10nsec. Output load is 1 TTL gate.

AC CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V$;(8) $V_{GG} = -12V \pm 5\%$, $V_{ILC} = 0.4V$ to $4.0V$

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
FREQUENCY	CLOCK REP RATE	DC	3	2	MHz	See Max Frequency Curve
$t_{\phi PW}$	CLOCK PULSE WIDTH	.300		100	μsec	
$t_{\overline{\phi}PW}$	$\overline{\text{CLOCK}}$ PULSE WIDTH	.200		DC	μsec	
t_R, t_F	CLOCK PULSE TRANSITION			5	μsec	
t_{DS}	DATA WRITE (SET-UP) TIME	100			nsec	
t_{DH}	DATA TO CLOCK HOLD TIME	50			nsec	
t_A	CLOCK TO DATA OUT DELAY		300	350	nsec	
t_{RS}	RECIRCULATE SET-UP TIME	150			ns	
t_{RH}	RECIRCULATE HOLD TIME	50			ns	
$t_{\overline{\phi}PW}$	$\overline{\text{CLOCK}}$ PULSE WIDTH	.200		DC	μsec	
C_{in}	INPUT CAPACITANCE		5	7	pF	@ 1MHz; $V_{in} = V_{CC}$; $V_{AC} = 25mV$ p-p
C_{ϕ}	CLOCK CAPACITANCE		6	7	pF	@ 1MHz; $V_{\phi} = V_{CC}$; $V_{AC} = 25mV$ p-p
V_{OL}	OUTPUT "LOW" VOLTAGE		0.4		V	Note 9
V_{OH}	OUTPUT "HIGH" VOLTAGE	3.6			V	$R_L = 7.5K\Omega$ to V_{GG}



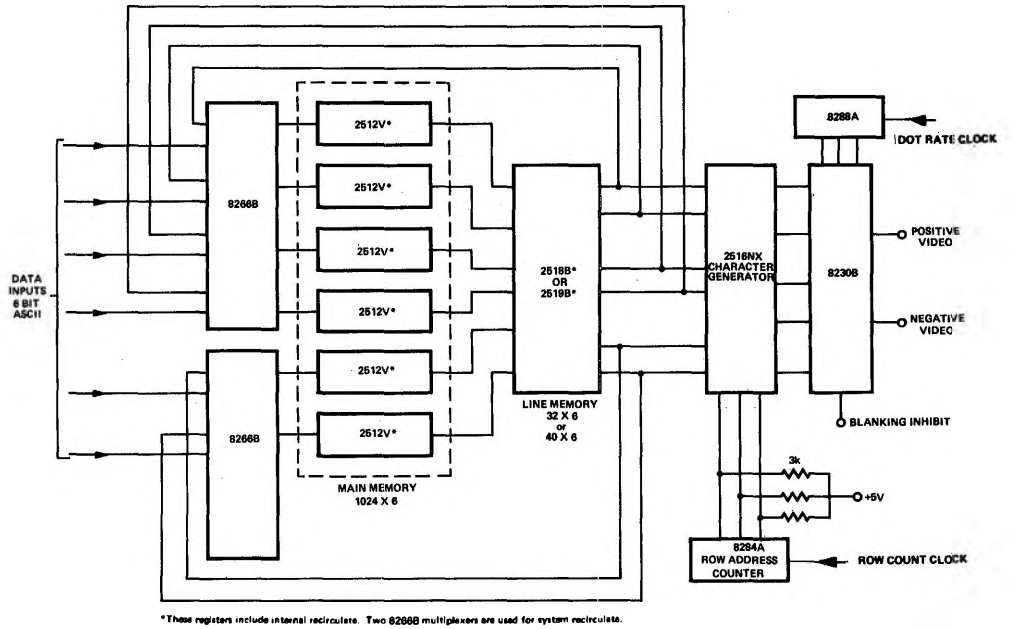
TTL INTERFACE



MOS INTERFACE

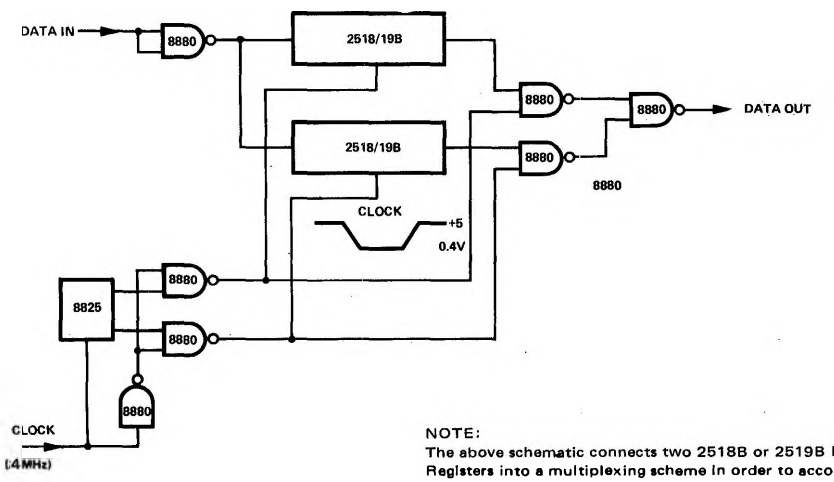
APPLICATIONS DATA

32 or 40 POSITION CRT DISPLAY MEMORY SYSTEM



*These registers include internal recirculate. Two 8266B multiplexers are used for system recirculate.

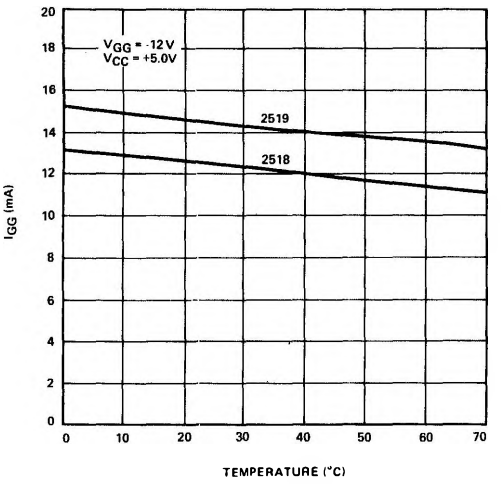
MULTIPLEXING LINE MEMORY REGISTERS AT 4MHz DATA RATE



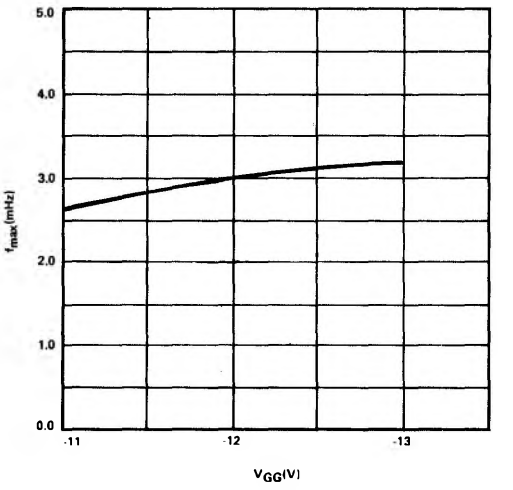
NOTE:
The above schematic connects two 2518B or 2519B Hex Shift Registers into a multiplexing scheme in order to accomplish a 64 or 80 character/line display at 4MHz data rate..

CHARACTERISTIC CURVES

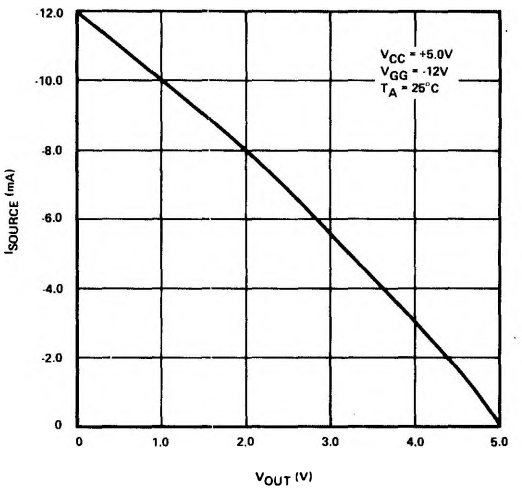
I_{GG} VERSUS TEMPERATURE



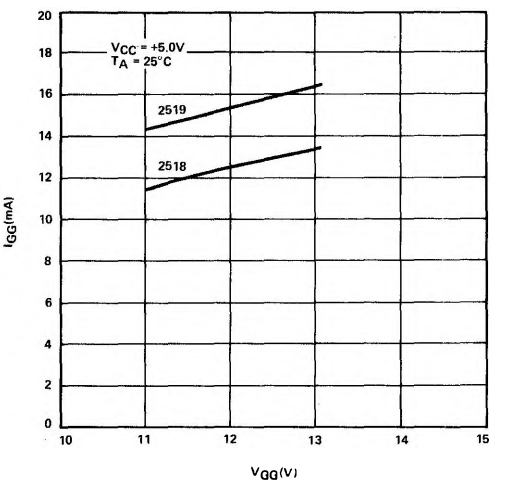
MAXIMUM SHIFT FREQUENCY VERSUS V_{GG}



I_{SOURCE} VERSUS V_{OUT}



I_{GG} VERSUS V_{GG}



CIRCUIT SCHEMATIC