DESCRIPTION

The 2521 128-bit and the 2522 132-bit recirculating static shift registers consist of enhancement mode p-channel silicon gate MOS devices integrated on a single monolithic chip.

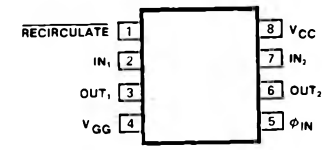
TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

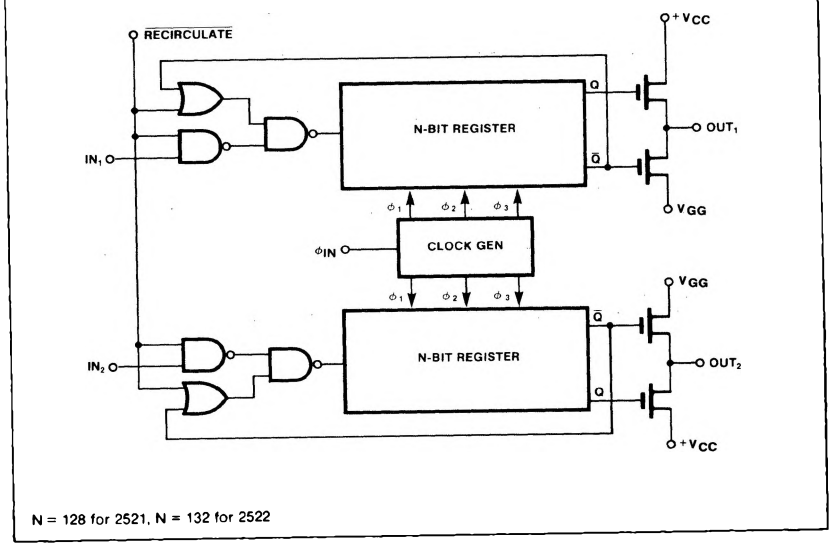
"0" = 0V, "1" = +5V.

PIN CONFIGURATION

N PACKAGE



BLOCK DIAGRAM



N = 128 for 2521, N = 132 for 2522

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range[2]		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at T_A = 70°C	535	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}	0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5V ± 5%, V_{GG} = −12V ± 5% unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[3]					V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
V_{ILC}	Clock low				0.6	
V_{IHC}	Clock high		3.4		5.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.5	
V_{OH}	High	I_{OH} = 100μA	3.8			
I_{LI}	Input load current	V_{IN} = 5.5V, T_A = 25°C		10	500	nA
I_{LC}	Clock leakage current	V_{ILC} = GND, T_A = 25°C		10	500	nA
I_{GG}	Supply current	Continuous operation, T_A = 25°C, f = 1.5MHz		28	32	mA
	Capacitance	At 1MHz, V_{AC} = 25mV p-p				pF
C_{IN}	Input	V_{IN} = V_{CC}			5	
C_ϕ	Clock	V_ϕ = V_{CC}			5	

AC ELECTRICAL CHARACTERISTICS

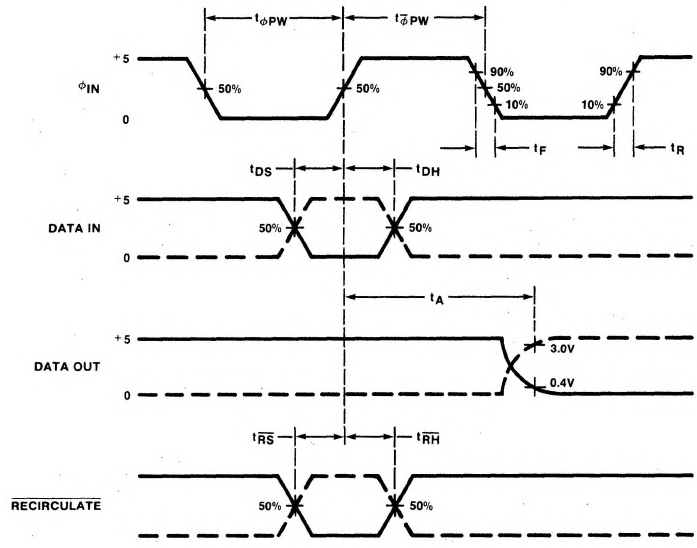
V_{CC} = 5V + 5V ± 5%, V_{GG} = −12V ± 5%, T_A = 0°C to 70°C

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Freq.	Clock rep rate				dc		1.5	MHz
	Pulse width			See timing diagram note				
$t_{\phi PW}$	Clock				.350	.100	100	μs
$t_{\overline{\phi} PW}$	$\overline{\text{Clock}}$				.200		dc	μs
t_R, t_F	Clock pulse transition[2]						1	μs
	Setup and hold time							ns
t_{DS}	Setup time	Write	Data		75			
t_{DH}	Hold time	Clock	Data		70			
$t_{\overline{RS}}$	Setup[2]	ϕ in high	$\overline{\text{Recirculate}}$		50			
$t_{\overline{RH}}$	Hold[2]	$\overline{\text{Recirculate}}$	ϕ in high					
t_A	Delay time[2]	Data	ϕ in high			250	350	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} − 1.85V and V_{IL} = V_{CC} − 4.15V.
4. All inputs are protected against static charge.
5. Parameters are valid over operating temperature range unless specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserving the right to make design and process changes and improvements.
8. Typical values are at +25°C and typical supply voltages.

TIMING DIAGRAM



NOTES

A. $t_R = t_F < 10ns$ for all inputs.
B. For static operation, clock must be stopped in TTL high state in order to retain data (see clock pulse width specification).