# DUAL 128-132 BIT STATIC 2521 SHIFT REGISTERS

2522

## SILICON GATE MOS 2500 SERIES

PIN CONFIGURATION (Top View)

#### DESCRIPTION

These Signetics 2500 Series Dual 128 and 132 bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

#### **FEATURES**

- PUSH-PULL OUTPUTS
- TTL/DTL COMPATIBLE CLOCK **PROVIDES** EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- TWO BIT LENGTHS AVAILABLE
- HIGH FREQUENCY OPERATION 2MHz TYPICAL **CLOCK RATE**
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGE 8 LEAD SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS **TECHNOLOGY**

#### **APPLICATIONS**

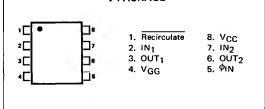
LOW COST SEQUENTIAL ACCESS MEMORIES LOW COST STATIC BUFFER MEMORIES CRT REFRESH MEMORIES - LINE STORAGE LINE PRINTERS **CASSETTE RECORDERS** 

#### BIPOLAR COMPATIBILITY

The clock and signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits.

### **BLOCK DIAGRAM**

# **V PACKAGE**



#### TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"O" is Written
1	1	"1" is Written

NOTE: "0" = 0V; "1" = +5V.

#### PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE		
2521V	Dual 128	8 Pin DIP		
2522V	Dual 132	8 Pin DIP		

#### **MAXIMUM GUARANTEED RATINGS (1)**

Operating Ambient Temperature (2) 0°C to +70°C

Storage Temperature -65°C to +150°C

Package Power Dissipation

at  $T_A = 70^{\circ} C$  535 mW

Data and Clock Input Voltages and Supply Voltages with respect to V<sub>CC</sub>

+0.3V to -20V

#### NOTES:

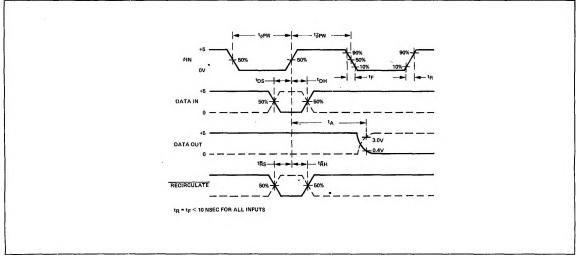
- Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and athermal resistance of 150°C/W junction to ambient.
- 3. All inputs are protected against static charge.
- Parameters are valid over operating temperature range unless specified.
- 5. All voltage measurements are referenced to ground.
- Manufacturer reserving the right to make design and process changes and improvements.
- 7. Typical values are at +25°C and nomin, supply voltages.
- V<sub>CC</sub> tolerance is ±5%. Any variation in actual V<sub>CC</sub> will be tracked directly by V<sub>1L</sub>, V<sub>1H</sub>, and V<sub>OH</sub> which are stated for a V<sub>CC</sub> of exactly 5 volts.

**DC CHARACTERISTICS**  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ;  $V_{CC} = +5V(8)$ ;  $V_{GG} = -12V \pm 5\%$  unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
ILI ILC IGG	INPUT LOAD CURRENT CLOCK LEAKAGE CURRENT POWER SUPPLY CURRENT		10 10 28	500 500 32	nÆ nA mA	$V_{in}$ = 5.5V, $T_A$ = 25°C $V_{ILC}$ = GND, $T_A$ = 25°C CONTINUOUS OPERATION $F$ = 1.5MHz, $T_A$ =25°C
V <sub>IL</sub>	INPUT "LOW" VOLTAGE	3.2		1.05 5.3	v v	F = 1,5MH2, 14=20 0
VILC	CLOCK INPUT "LOW" VOLTAGE			1,05	v	
VIHC	CLOCK INPUT "HIGH" VOLTAGE	3.2		5.43	· v	

CONDITIONS OF TEST Input rise and fall times: 10 nsec. Output load is 1 TTL gate

#### **TIMING DIAGRAM**

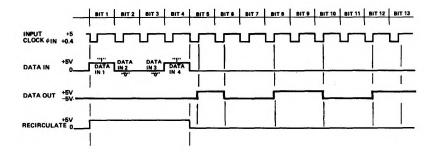


AC CHARACTERISTICS  $\vec{V}_{CC}$  = +5V (8);  $V_{GG}$  = -12V ±5%,  $V_{IC}$  = 0.4 to 4.0;  $T_A$ =0° to +70°C

SYMBOL	TEST	MIN	ТҮР	мах	UNIT	CONDITIONS
FREQUENCY	CLOCK REP RATE	DC		1.5	MHz	See Maximum Frequency Curve
$^{t}\phi_{PW}$	CLOCK PULSE WIDTH	.350	.100	100	Msec	
t o PW	CLOCK PULSE WIDTH	.200		DC	μsec	
t <sub>R</sub> , t <sub>E</sub>	CLOCK PULSE TRANSITION			1	usec	
tDS	DATA WRITE (SET-UP) TIME	75	i i		nsec	
<sup>t</sup> DH	DATA TO CLOCK HOLD TIME	50			nsec	
<sup>t</sup> A	CLOCK TO DATA OUT DELAY		250	350	nsec	
<sup>t</sup> RS	RECIRCULATE SET-UP TIME	50			ns	
<sup>t</sup> RH	RECIRCULATE HOLD TIME	50	<b>{</b>	_	ns	
CIN	INPUT CAPACITANCE			5	pF	@ 1MHz; V <sub>in</sub> = V <sub>CC</sub> ;
		1	1			V <sub>AC</sub> = 25mV p-p
$c\phi$	CLOCK CAPACITANCE			5	pF	@ 1MHz; $V_{\phi} = V_{CC}$ ;
		1	ł			$V_{AC} = 25 \text{mV p-p}$
$v_{OL}$	OUTPUT "LOW" VOLTAGE	-4.0		0.4	v	1 TTL load (IL=1.6mA)
$v_{OHI}$	OUTPUT "HIGH" VOLTAGE	ł	1			
	DRIVING 1 TTL LOAD	3,0	3.5		v	1 TTL load (I <sub>I</sub> = 100 <i>μ</i> Α)
VoH2	OUTPUT "HIGH" VOLTAGE	ľ	<b>\</b>			
	DRIVING MOS	3.5	4.0		V	

#### **TIMING DIAGRAM**



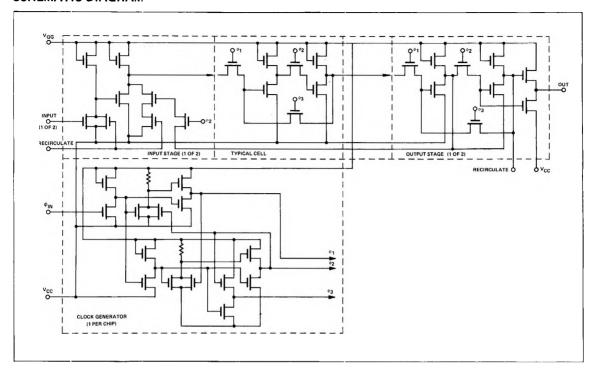


NOTE 1: WRITE CYCLE The positive going edge of the recirculative control is coincident with the negative going edge of the input clock  $(\phi_{1N})$ .

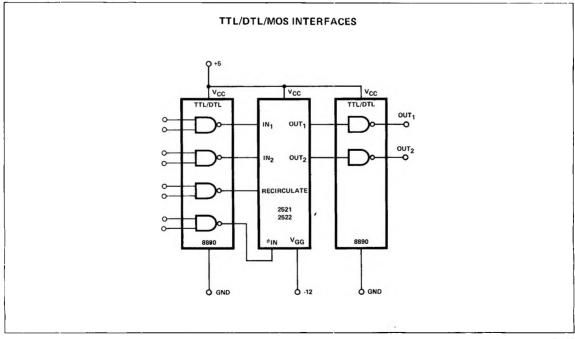
\*For clarity, a four bit hypothetical example is shown

NOTE 2: RECIRCULATE CYCLE Data recirculates if the recirculate control is a "0"

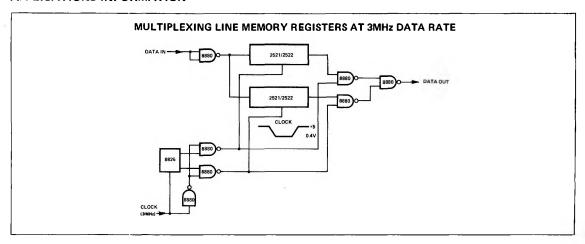
# SCHEMATIC DIAGRAM



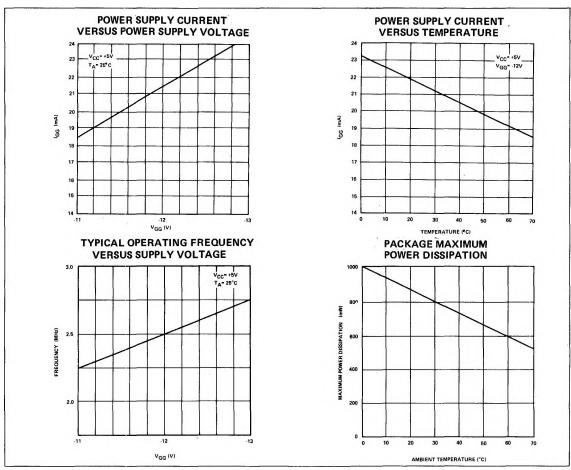
# **APPLICATIONS DATA**



#### APPLICATIONS INFORMATION



#### **CHARACTERISTIC CURVES**



# 132 COLUMN LINE PRINTER

