

DUAL 240-BIT STATIC SHIFT REGISTER (240X2)
DUAL 250-BIT STATIC SHIFT REGISTER (250X2)
DUAL 256-BIT STATIC SHIFT REGISTER (256X2)

2527
2528
2529

2527-N • 2528-N • 2529-N

DESCRIPTION

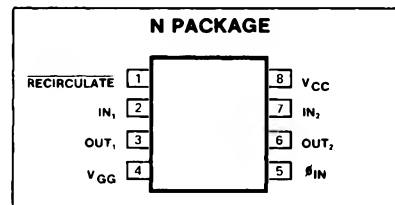
The 2527 240-bit, 2528 250-bit, and the 2529 256-bit recirculating static shift registers consist of enhancement mode p-channel silicon gate MOS devices integrated on a single monolithic chip.

TRUTH TABLE

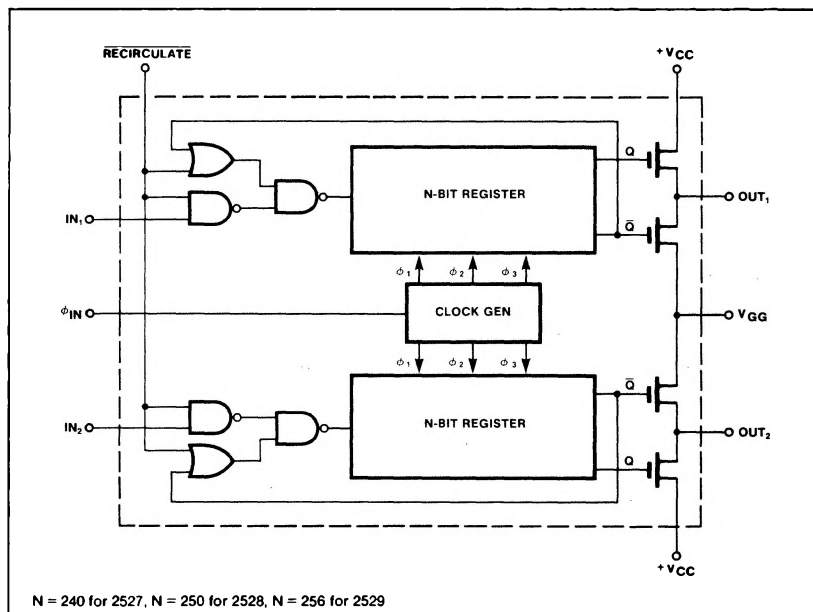
RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

"0" = 0V; "1" = +5V

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING	UNIT
T_A Temperature range ²		°C
Operating	0 to 70	
T_{STG} Storage	-65 to 150	
P_D Power dissipation at $T_A = 70^\circ\text{C}$	535	mW
Data and clock input voltages and supply voltages with respect to V_{CC}	0.3 to -20	V

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DC ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{GG} = -12\text{V} \pm 5\%$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Input voltage ³					V
V_{IL} Low				0.6	
V_{IH} High		3.4		5.3	
V_{ILC} Clock low				0.6	
V_{IHC} Clock high		3.4		5.3	
Output voltage					V
V_{OL} Low	$I_{OL} = 1.6\text{mA}$			0.5	
V_{OH} High	$I_{OH} = 100\mu\text{A}$	3.8			
I_{LI} Input load current	$V_{IN} = 5.5\text{V}$, $T_A = 25^\circ\text{C}$		10	500	nA
I_{LC} Clock leakage current	$V_{ILC} = 0\text{V}$, $T_A = 25^\circ\text{C}$		10	500	nA
I_{GG} Supply current	Continuous operation, $T_A = 25^\circ\text{C}$, $f = 1.5\text{MHz}$, Outputs open		28	35	mA
Capacitance					pF
C_{IN} Input	At 1MHz, $V_{AC} = 25\text{mV p-p}$ $V_{IN} = V_{CC}$			5	
C_ϕ Clock	$V_\phi = V_{CC}$			5	

AC ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{GG} = -12\text{V} \pm 5\%$,

Input rise and fall times = 10ns, Output load = 1TTL gate.

PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Freq. Clock rep rate			See timing diagram note	dc	2.5	1.5	MHz
Pulse width							μs
$t_{\phi PW}$ Clock				0.2	0.1	100	
$t_{\phi PW}$ Clock				0.2		dc	
t_R, t_F Clock pulse transition						1	μs
Setup and hold time							ns
t_{DS} Setup time	ϕ_{in}	Data in		50			
t_{DH} Hold time	Data in	ϕ_{in}		70			
t_{RS} Setup time	ϕ_{in}	Recirculate		50			
t_{RH} Hold time	Recirculate	ϕ_{in}					
t_A Delay time	Data out	Clock	$I_{OL} = 1.6\text{mA}$		330	450	ns

NOTES

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated based on a $+150^\circ\text{C}$ maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
- Guaranteed input levels are stated for worst case conditions including a $\pm 5\%$ variation in V_{CC} and a temperature variation of $0^\circ\text{C to } +70^\circ\text{C}$. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85\text{V}$ and $V_{IL} = V_{CC} - 4.15\text{V}$.
- All inputs are protected against static charge.
- Parameters are valid over operating temperature range unless specified.
- All voltage measurements are referenced to ground.
- Manufacturer reserves the right to make design and process changes and improvements.
- Typical values are at $+25^\circ\text{C}$ and typical supply voltages.

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TIMING DIAGRAM

