2527-N • 2528-N • 2529-N

DESCRIPTION

The 2527 240-bit, 2528 250-bit, and the 2529 256-bit recirculating static shift registers consist of enhancement mode p-channel silicon gate MOS devices integrated on a single monolithic chip.

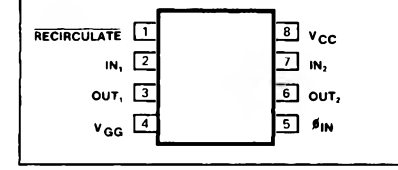
TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

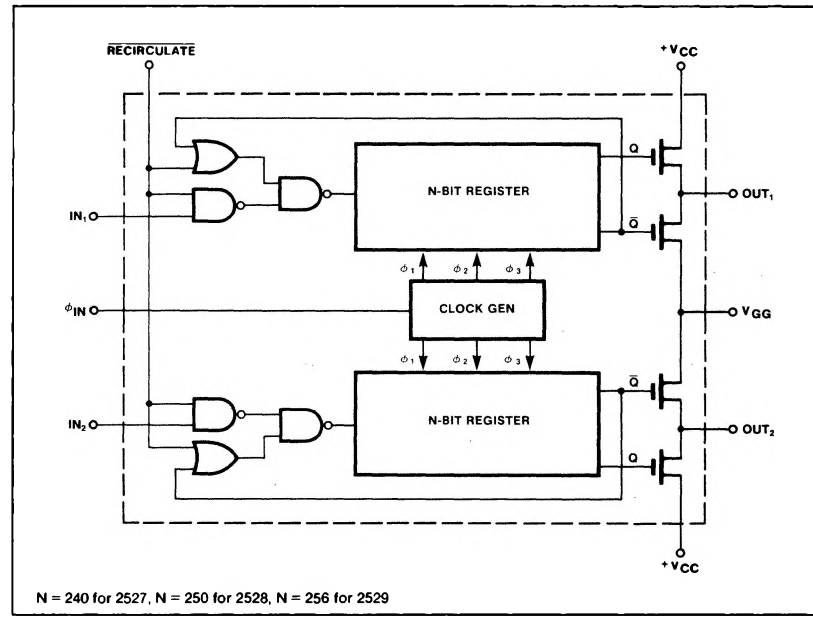
"0" = 0V; "1" = +5V

PIN CONFIGURATION

N PACKAGE



BLOCK DIAGRAM



N = 240 for 2527, N = 250 for 2528, N = 256 for 2529

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range[2]		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at T_A = 70°C	535	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}	0.3 to -20	V

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DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{GG} = -12V \pm 5\%$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[3]					V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
V_{ILC}	Clock low				0.6	
V_{IHC}	Clock high		3.4		5.3	
	Output voltage					V
V_{OL}	Low	$I_{OL} = 1.6mA$			0.5	
V_{OH}	High	$I_{OH} = 100\mu A$	3.8			
I_{LI}	Input load current	$V_{IN} = 5.5V$, $T_A = 25°C$		10	500	nA
I_{LC}	Clock leakage current	$V_{ILC} = OV$, $T_A = 25°C$		10	500	nA
I_{GG}	Supply current	Continuous operation, $T_A = 25°C$, f = 1.5MHz, Outputs open		28	35	mA
	Capacitance	At 1MHz, $V_{AC} = 25mV$ p-p				pF
C_{IN}	Input	$V_{IN} = V_{CC}$			5	
C_ϕ	Clock	$V_\phi = V_{CC}$			5	

AC ELECTRICAL CHARACTERISTICS

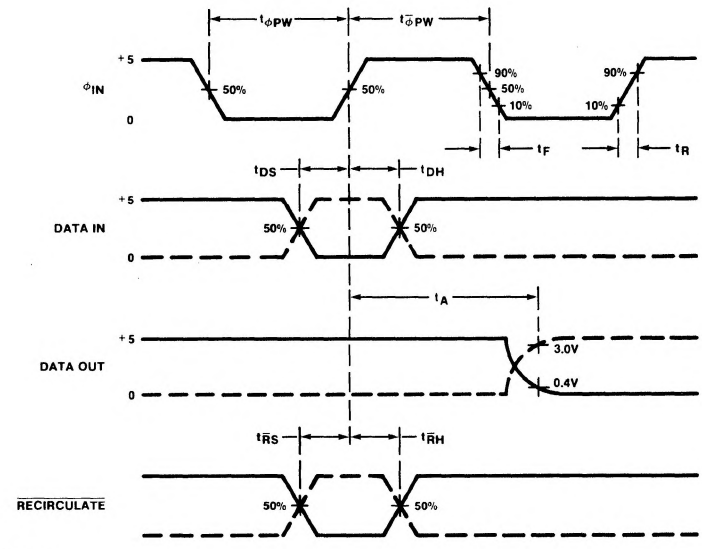
$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{GG} = -12V +5\%$,
Input rise and fall times = 10ns, Output load = 1TTL gate.

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Freq.	Clock rep rate			See timing diagram note	dc	2.5	1.5	MHz
	Pulse width							μs
$t_{\phi PW}$	Clock				0.2	0.1	100	
$t_{\overline{\phi} PW}$	$\overline{\text{Clock}}$				0.2		dc	
$t_{R,tF}$	Clock pulse transition						1	μs
	Setup and hold time							ns
t_{DS}	Setup time	ϕin	Data in		50			
t_{DH}	Hold time	Data in	ϕin		70			
$t_{\overline{RS}}$	Setup time	ϕin	$\overline{\text{Recirculate}}$		50			
t_{RH}	Hold time	$\overline{\text{Recirculate}}$	ϕin					
t_A	Delay time	Data out	Clock	$I_{OL} = 1.6mA$		330	450	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.
4. All inputs are protected against static charge.
5. Parameters are valid over operating temperature range unless specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at +25°C and typical supply voltages.

TIMING DIAGRAM



NOTES

A. $t_R = t_F < 10$ns for all inputs.
B. For static operation, the input clock must be stopped in the TTL high state in order to retain data (see clock pulse width specification).