signetics

DUAL 256-250-240 BIT STATIC SHIFT REGISTERS

PRELIMINARY SPECIFICATION

SILICON GATE 2500 SERIES

2527
2528
2529

DESCRIPTION

The Signetics 2500 Series Dual 256, 250 and 240 bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

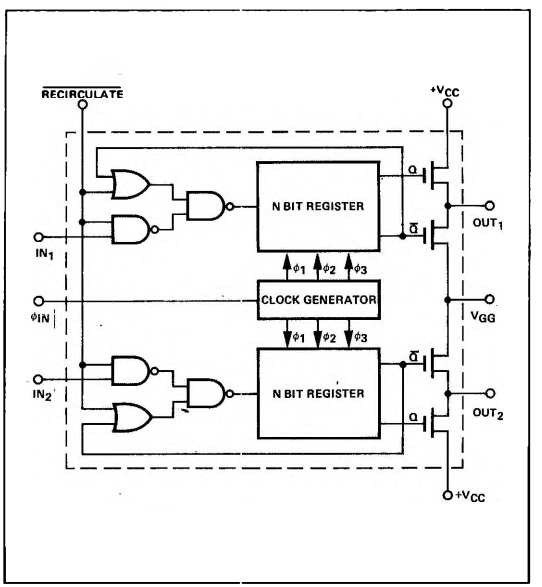
FEATURES

- PUSH-PULL OUTPUTS
- TTL/DTL COMPATIBLE CLOCK – PROVIDES EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- THREE BIT LENGTHS AVAILABLE
- HIGH FREQUENCY OPERATION – 3 MHz TYPICAL CLOCK & DATA RATE
- TTL, DTL COMPATIBLE INPUTS AND OUTPUTS
- STANDARD PACKAGE – 8 LEAD SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
DELAY LINES
CASSETTE RECORDERS

BLOCK DIAGRAM

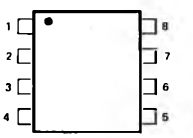


BIPOLAR COMPATIBILITY

The clock and signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The outputs drive directly into TTL/DTL without requiring external resistors.

PIN CONFIGURATION (Top View)

V PACKAGE



1. $\overline{\text{Recirculate}}$
2. IN_1
3. OUT_1
4. V_{GG}
8. V_{CC}
7. IN_2
6. OUT_2
5. ϕ_{IN}

TRUTH TABLE

$\overline{\text{RECIRCULATE}}$	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

NOTE: "0" = 0V; "1" = +5V

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2527V	Dual 256	8 Pin DIP
2528V	Dual 250	8 Pin DIP
2529V	Dual 240	8 Pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation at T_A = 70°C	535 mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to -20V

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V(8); V_{GG} = -12V ±5% unless otherwise noted.

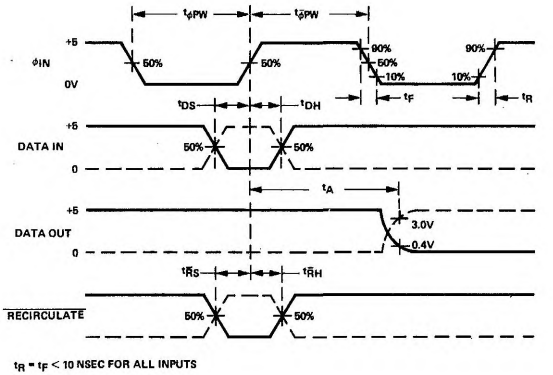
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = 5.5V, T_A = 25°C
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = 0V, T_A = 25°C
I_{GG}	Power Supply Current		28	35	mA	Continuous Operation F = 2.5 MHz, T_A = 25°C Outputs Open
V_{IL}	Input "Low" Voltage			1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage			1.05	V	
V_{IHC}	Clock Input "High" Voltage	3.2		5.3	V	

AC CHARACTERISTICS T_A =0° to +70°C, V_{CC} = +5V(8); V_{GG} = -12V +5%, V_{IC} = 0,4 to 4.0V

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
FREQUENCY	Clock Rep Rate	DC	2.5	1.5	MHz	See Maximum Frequency Curve
$t_{\phi PW}$	Clock Pulse Width	0.2	0.1	100	μs	
$t_{\overline{\phi}PW}$	$\overline{\text{Clock}}$ Pulse Width	0.2		DC	μs	
t_R t_F	Clock Pulse Transition			1	μs	
t_{DS}	Data Set-up Time	50			ns	
t_{DH}	Data Hold Time	50			ns	
t_A	Clock to Data Out Delay		330	450	ns	I_{OL} = 1.6mA
$t_{\overline{R}S}$	$\overline{\text{Recirculate}}$ Set-up Time	50			ns	
$t_{\overline{R}H}$	$\overline{\text{Recirculate}}$ Hold Time	50			ns	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz; V_{IN} = V_{CC}; V_{AC} = 25mV p-p
C_ϕ	Clock Capacitance			5	pF	@ 1 MHz; V_ϕ = V_{CC}; V_{AC} = 25mV p-p
V_{OL}	Output "Low" Voltage			0.4	V	1 TTL load (I_L = 1.6mA)
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	3.0	3.5		V	1 TTL load (I_I = 100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.5	4.0		V	

CONDITIONS OF TEST Input rise and fall times: 10 nsec. Output load is 1 TTL gate.

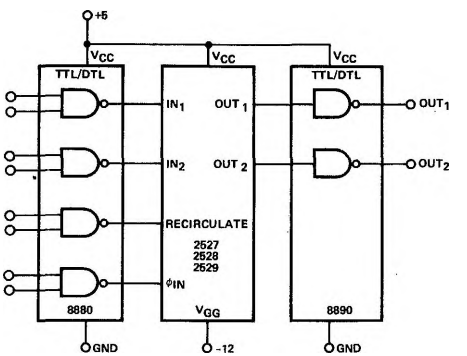
TIMING DIAGRAM



$t_R = t_F < 10$ NSEC FOR ALL INPUTS

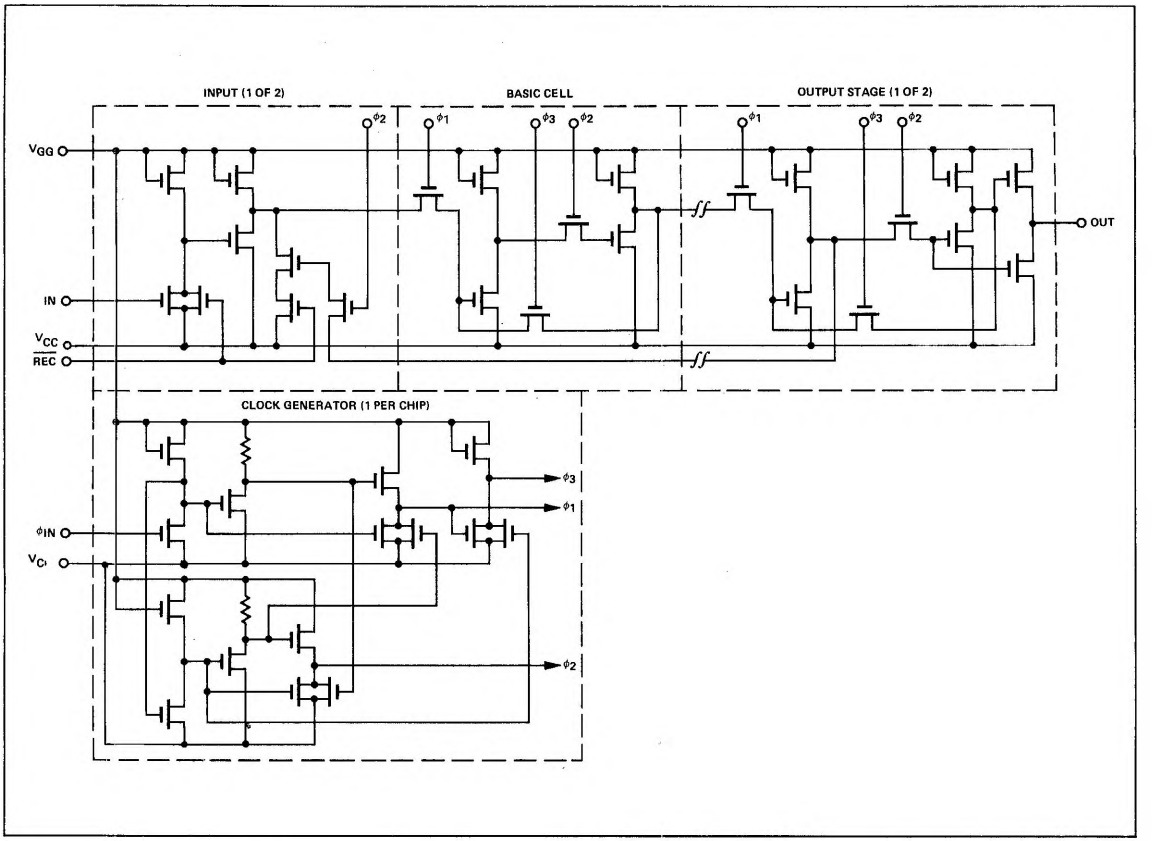
APPLICATIONS INFORMATION

TTL/DTL/MOS INTERFACES

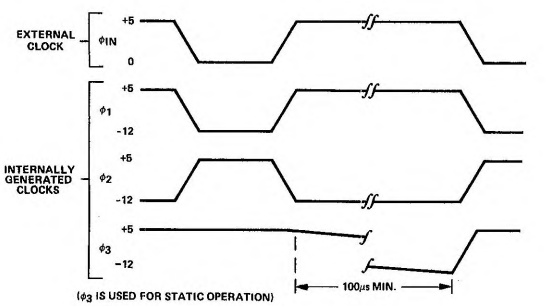


Note: When using 7400 series data, recirculate and clock drivers, connect 10k resistor from driver output to V_{CC}. This insures an adequate "1" level input for the MOS register. See page 13 of MOS Handbook.

SCHEMATIC DIAGRAM

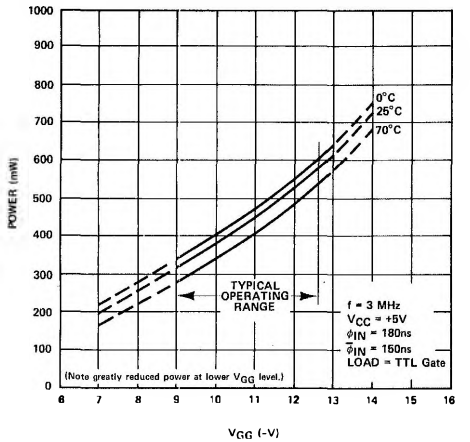


CLOCKING WAVEFORMS

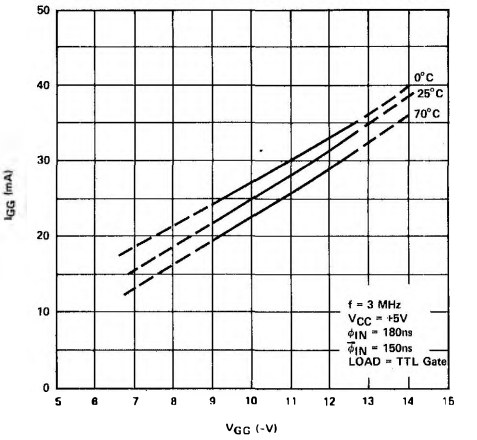


CHARACTERISTIC CURVES

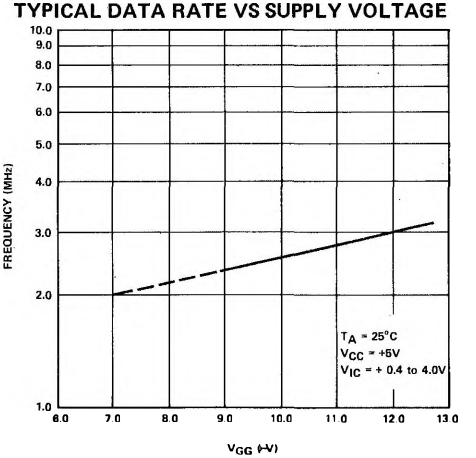
POWER DISSIPATION VS SUPPLY VOLTAGE



SUPPLY CURRENT VS SUPPLY VOLTAGE

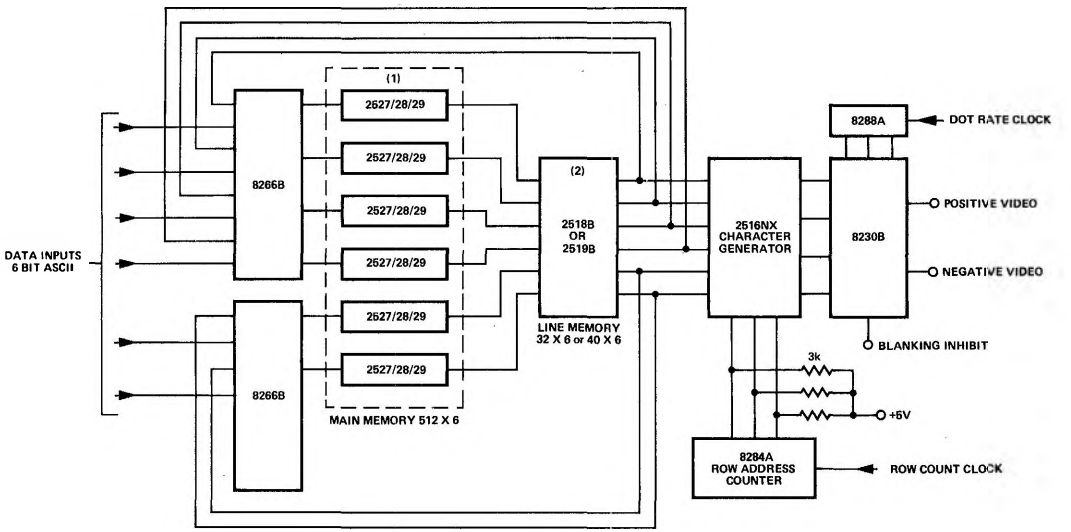


TYPICAL DATA RATE VS SUPPLY VOLTAGE



APPLICATIONS INFORMATION (Cont'd)

12 LINE, 32 OR 40 CHARACTER PER LINE CRT DISPLAY MEMORY SYSTEM



(1) Duals connected in series.
(2) These registers include internal recirculate. Two 8266B multiplexers are used for system recirculate.