Signetics

FULLY DECODED, 2048-BIT RANDOM ACCESS MEMORY 2548

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2548 2048x1 Dynamic Random Access Memory employs enhancement mode P-channel devices integrated on a single monolithic chip. The device is fully decoded and contains built-in refresh amplifiers. All address input data and control lines are directly TTL compatible. Clocking is performed by three high level (0V to -20V) nonoverlapping clock inputs. (Use Signetics N575 Clock Driver.) The output data line supplies a minimum "1" level output of 600μA. (Use Signetics 8T25 Sense Amplifier.)

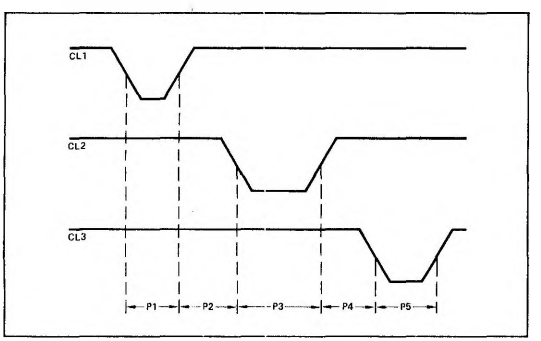
FEATURES

- HIGH STORAGE DENSITY
- READ ACCESS TIME 345ns MAX.
- READ/WRITE CYCLE TIME 560ns MAX.
- REFRESH PERIOD – 2mS FOR 0°C TO 70°C AMBIENT
- AUTOMATIC REFRESH OF A 64 BIT COLUMN DURING EACH READ
- LOW POWER DISSIPATION 150μW/BIT MAX. (AT 1.8MHz)
- STANDBY POWER 2μW/BIT MAX.
- STANDARD 22 PIN DIP PACKAGE, 400 MIL ROW SPACING
- V_{CC} = 5V, V_{BB} = 8.5V, V_{DD} = –15V
- ALL INPUTS EXCEPT CL1, CL2, CL3 ARE TTL COMPATIBLE
- ADDRESS AND CHIP SELECT INPUT LATCHES PROVIDED ON CHIP
- CHIP SELECT PERMITS SIMPLE MEMORY EXPANSION

APPLICATIONS

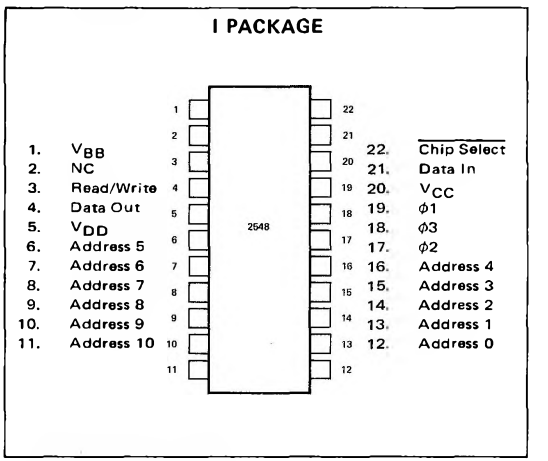
CORE MEMORY REPLACEMENT
DOUBLED STORAGE CAPACITY (OVER 1K RAMS)
BUFFER STORES
MAIN MEMORY

GENERAL TIMING AND OPERATION



PIN CONFIGURATION (TOP VIEW)

I PACKAGE



BIPOLAR COMPATIBILITY

All address lines, control lines and data input lines are directly TTL compatible and defined in positive logic. The three clocks require high level drivers. The data out line is a non-inverted current source output requiring a sense amplifier or high impedance gate. (Signetics N575 Clock Driver and 8T25 Sense Amplifier are recommended.)

GENERAL TIMING AND OPERATION

1. During period 1 internal nodes are precharged. The rising edge of CL1 (end of Period 1) clocks input address and CS data into storage elements.
2. During period 2 the row and column decoders select the desired bit.
3. During period 3 the information in the bit is exclusive OR'd with the selected information contained in the column inversion memory. The result is sent to the output. The output information is stable near the end of period 3.
4. During period 4 the write enable circuitry is activated. The internal data-in level is determined by exclusive OR'ing the actual input with the selected information contained in the column inversion memory.
5. If a write is desired during period 5, data is written into the selected bit. The information stored in all other bits sharing the same addressed column is inverted and refreshed. The appropriate bit of the column inversion memory is also inverted and refreshed.

   If a refresh is desired during period 5, the information stored in all bits sharing the same addressed column is inverted and refreshed. The appropriate bit of the column inversion memory is also inverted and refreshed.

PART IDENTIFICATION

TYPE	PACKAGE	OP. TEMP. RANGE
2548I	22-Pin Ceramic DIP (0.4")	0–70°C
2548XC	22-Pin Plastic DIP	0–70°C

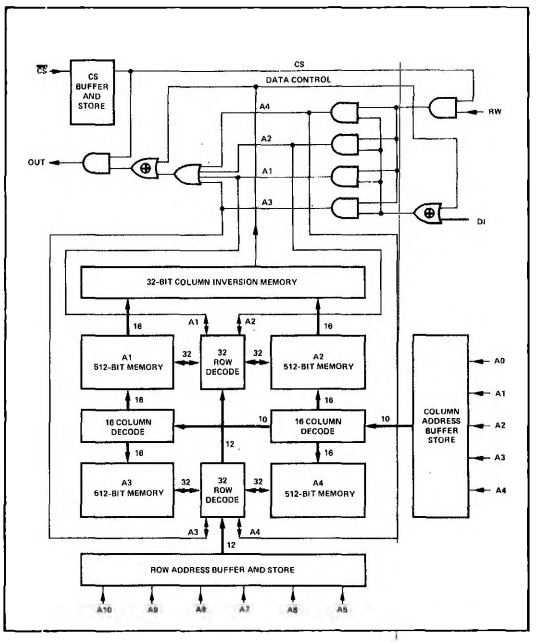
NOTE: "0" = 0 V, "1" = +5 V

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	−65°C to 150°C
All Input or Output Voltage with respect to the most positive supply V_{BB}	+0.3 V to −25 V
Supply Voltages with respect to V_{BB}	+0.3 V to −25 V
Package Power Dissipation at T_A = 25°C	800 mW

NOTES:
1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. The V_{BB} supply should be applied at or before the V_{CC} supply.
3. t_r and t_f = 20ns: for all inputs. All timing measurements are made at the 50% points.
4. Only CL1 and CL2 are required for a short read cycle. 60 ns after CL2 the next cycle can start. No refresh occurs when using short read cycles.

BLOCK DIAGRAM



DC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5 V, V_{BB} = 8.5 V ±0.5 V, V_{DD} = −15 ±1 V unless otherwise noted.(2)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LC}	Clock Load Current			5.0	μA	$V_{CLK} = V_{DD}$
I_{LI}	Input Load Current			1.0	μA	$V_{IN} = V_{DD}$
						CL1 = V_{DD}
I_{LO}	Output Leakage Current			1.0	μA	$V_{OUT} = V_{DD}$, CL2 = V_{CC}
						CL3 = V_{CC}
I_{DD}	Average Power Supply Current			10.0	mA	T_A = 25°C, T_{cyc} = 560 ns
I_{BB}	Average Power Supply Current			500.0	μA	T_A = 25°C, T_{cyc} = 560 ns
V_{IL}	Input Low Voltage	V_{DD} −1.0		V_{CC} −4.5	V	
V_{IH}	Input High Voltage	V_{CC} −1.5		V_{CC}	V	
V_{ILC}	Clock Input Low Voltage	-16		-14	V	
V_{IHC}	Clock Input High Voltage	V_{CC} −1.5		V_{CC}	V	
I_{OH}	Output High Source Current	0.6			mA	R_L = 1.1 K connected to 0 V
I_{OL}	Output Low Source Current			25.0	μA	R_L = 1.1 K connected to 0 V
C_{ADD}	Address Input Capacitance			5.0	pF	
$C_{\overline{CS}}$	$\overline{CS}$ Input Capacitance			5.0	pF	
C_{RW}	R/W Input Capacitance			5.0	pF	$V_{IN} = V_{CC}$, = 1 MHz
C_{DI}	DI Input Capacitance			6.0	pF	
C_{CL1}	CL1 Input Capacitance			35.0	pF	
C_{CL2}	CL2 Input Capacitance			16.0	pF	
C_{CL3}	CL3 Input Capacitance			25.0	pF	
C_{OUT}	Output Capacitance			5.0	pF	$V_{CL1} = V_{DD}$, $V_{OUT} = V_{CC}$ $V_{CL2} = V_{CL3} = V_{CC}$, f = 1 MHz

AC CHARACTERISTICS [3]

T_A = 0°C to 70°C, V_{CC} = 5 V, V_{BB} = 8.5 V ±0.5 V, V_{DD} = −15 V ±1 V unless otherwise noted.[2]

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
General Memory Cycle Timing						
T_{REF}	Time Between Refresh			2.0	ms	
T_{1PW}	CL1 Pulse Width	75			ns	
T_{12}	CL1 to CL2 Gap	75			ns	
T_{2PW}	CL2 Pulse Width	240			ns	
T_{23}	CL2 to CL3 Gap	50			ns	
T_{3PW}	CL3 Pulse Width	70			ns	
T_{31}	CL3 to CL1 Gap	50			ns	
T_{AS}	Address & Chip Select Setup Time	40			ns	
T_{AH}	Address & Chip Select Hold Time	60			ns	
T_{OUT}	CL2 to Output Access Time	230			ns	R_L = 1.1 K, C_L = 30pF, V_{REF} = 500 μA
T_{CYC}	Cycle Time	560			ns	
T_{SRC} [4]	Short Read Cycle Time	450			ns	
T_{21} [4]	CL2 to CL1 Gap (for SRC only)	60			ns	
Read/Refresh Cycle Timing						
T_{ACC1}	CL1 to Output Access	380			ns	$T_{1PW} + T_{12} + T_{OUT}$
T_{ACC1}	Address or Chip Select to Output	345			ns	$T_{AS} + T_{12} + T_{OUT}$
T_{RWS3}	Read Setup Time	60			ns	
T_{RWH3}	Read Hold Time	20			ns	
Read/Write Cycle Timing						
T_{RWS2}	Write Setup Time	0			ns	
T_{DS1}	Data High Setup Time	100			ns	
T_{DS0}	Data Low Setup Time	60			ns	
T_{DH}	Data Hold Time	20			ns	

GENERAL NOTES:

A. Everytime a column is accessed during a normal memory cycle (either a READ or a WRITE, but not a SHORT READ), all 64 bits in that column are refreshed.

B. Refreshing continues to occur even if the device is not selected ($\overline{CS}$ = "1").

C. When $\overline{CS}$ = "1" the Data In and Read/Write inputs are disabled so that no data can be written into the device. When $\overline{CS}$ = "1", the output of the device is left floating so that many device outputs can easily be OR'ed together.

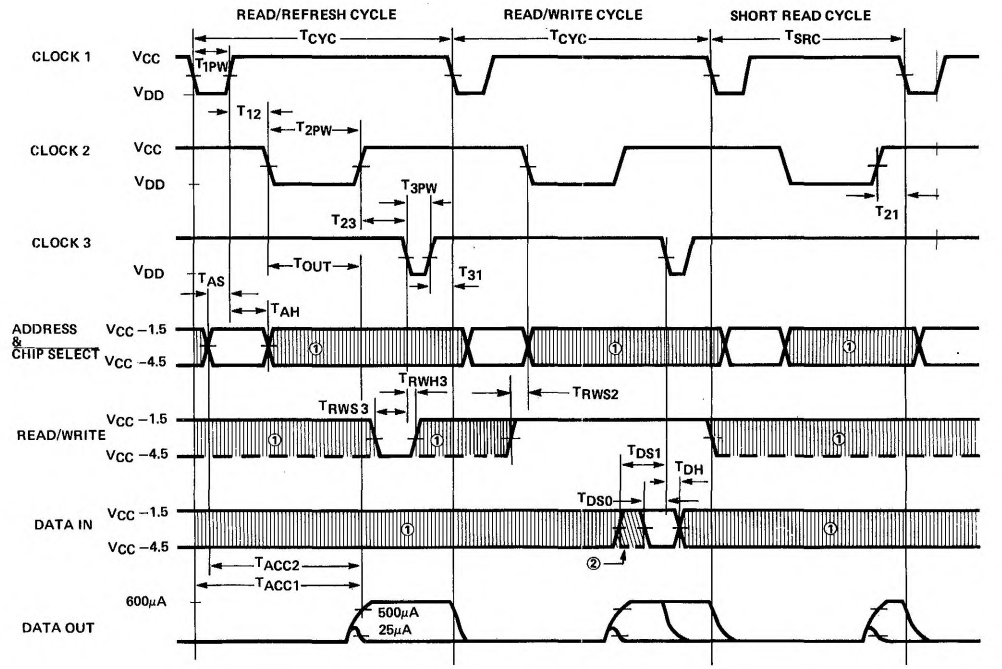
D. A_0 through A_4 are the column address lines. A_5 through A_{10} are the row address lines.

E. For proper refreshing, all column addresses (32 of them) must be selected at least once during every 2 ms period.

F. Inputs A_0 through A_{10} and $\overline{CS}$ are essentially clocked into the device on the rising edge of CL1. They are then held by internal latches for the duration of each memeory cycle.

G. The RAM is non-inverting such that data written in as a "1" (DI = "1") is read out as a positive current greater than 600 μA. Data written in as a "0" is read out as a very small current less than 25 μA.

TIMING DIAGRAM



NOTES:
1. Signal may change with no effect.
2. Data In can go low but cannot go high during this time.