signetics

8192- BIT HIGH SPEED STATIC READ-ONLY MEMORY 2580

PRELIMINARY SPECIFICATION

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The 2580 is a high speed 8,192 Static Read-Only Memory available in a 2048x4 organization. This device has TTL compatible inputs and outputs and requires +5V and -12V power supplies. A READ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing larger memories. The outputs are enabled by a programmable four bit select code applied to four binary chip select terminals.

FEATURES

- 2048x4 ORGANIZATION
- 625ns TYPICAL ACCESS TIME
- STATIC OPERATION, NO REFRESHING
- OUTPUT LATCHES
- BUILT-IN 1 OF 16 CHIP ENABLE DECODER
- TTL/DTL COMPATIBLE INPUTS
- TTL/DTL COMPATIBLE THREE-STATE OUTPUTS
- V_{CC} = +5V, V_{GG} = -12V, V_{DD} = 0V
- 24 PIN SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

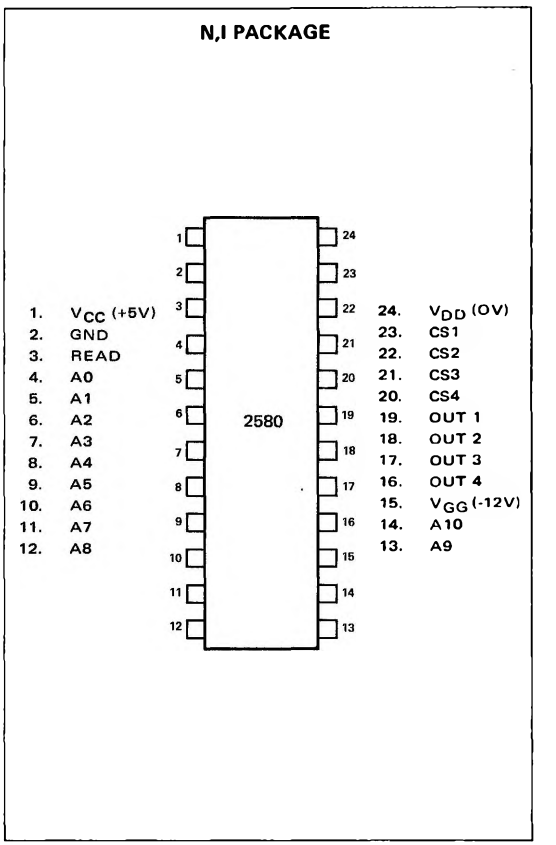
- MICRO-PROGRAMMING
- LOOK-UP TABLES
- CODE CONVERSION
- RANDOM LOGIC SYNTHESIS
- CHARACTER GENERATION

BIPOLAR COMPATIBILITY

All inputs of the 2580 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA sufficient to drive one standard TTL load.

PIN CONFIGURATION (Top View)

N,I PACKAGE

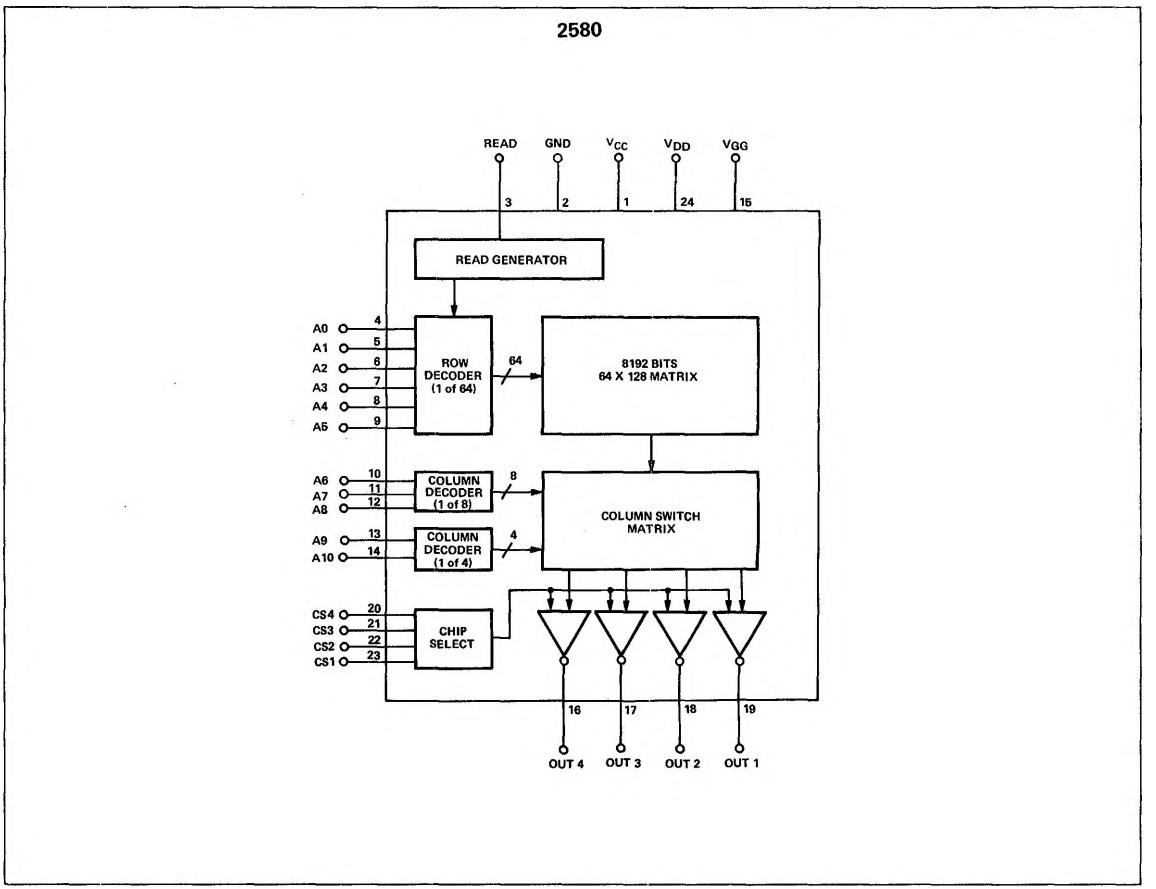


PART IDENTIFICATION

PART NUMBER	OP. TEMP. RANGE	PACKAGE
2580N	0-70°C	24-PIN DIP
2580I	0-70°C	24-PIN DIP

Note: "0" = 0V, "1" = +5V

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation[2] @ 70° C	730mW
Input[3] and Supply Voltages with respect to V_{CC}	+0.3 to -20V

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V ±5%, V_{DD} = 0V, V_{GG} = -12V ±5% unless otherwise noted. (See notes 4, 5, 6, 7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = 0V T_A = 25°C V_{CE} = V_{CC}
I_{CC}	V_{CC} Power Supply Current		23	35	mA	(8)
I_{GG}	V_{GG} Power Supply Current		23	35	mA	(8)
V_{IL}	Input Logic "0"			1.05	V	
V_{IH}	Input Logic "1"	3.2		5.3	V	

AC CHARACTERISTICS

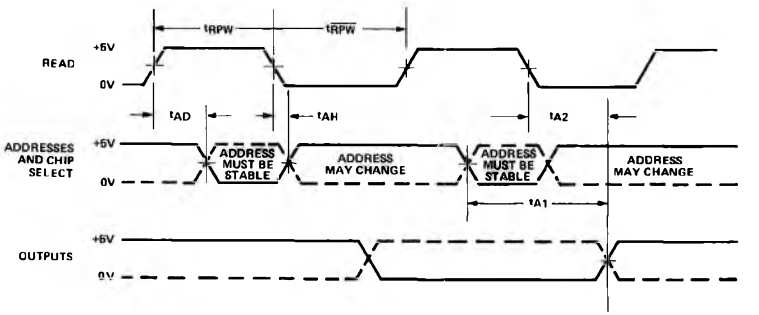
T_A = 25°C; V_{CC} = 5V ±5%, V_{DD} = 0V, V_{GG} = -12V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OL}	Output Logic "0"			0.8	V	One TTL Load
V_{OH}	Output Logic "1"	3.5			V	One TTL Load
t_{RPW}[10]	Read Pulse Width	500	400		ns	
t_{RPW}[9]	Read Pulse Width	500	400		ns	
t_{AD}	Address Delay Time (11)			50	ns	
t_{AH}	Address Hold Time	0			ns	
t_{A1}	Address to Output Delay		625	700	ns	
t_{A2}	End of Read Pulse to Output Delay		200	250		
C_{IN}	Input Capacitance			10	pF	f = 1MHz, V_{AC} = 25mV p-p V_{IN} = V_{CC}

NOTES:

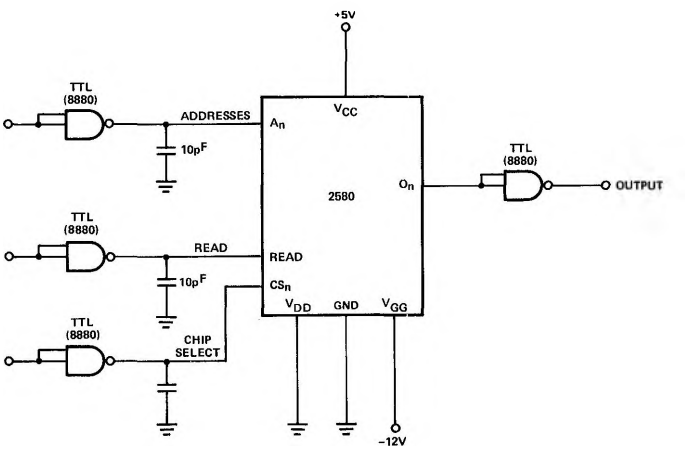
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Outputs open, t_{RPW} = 500ns, $t_{\overline{RPW}}$ = 500ns.
9. During $t_{\overline{RPW}}$ data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
10. During t_{RPW} addresses are decoded and sent to the memory matrix; and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (falling edge) of the READ pulse. After t_{A2}, data appears at the output terminals.
11. Addresses must be stable within 50ns after the READ line rises and must remain stable until the READ line falls.

TIMING DIAGRAM



Note: All measurements made at 50% points.
Input $t_r = t_f = 10ns$.

AC TEST SETUP

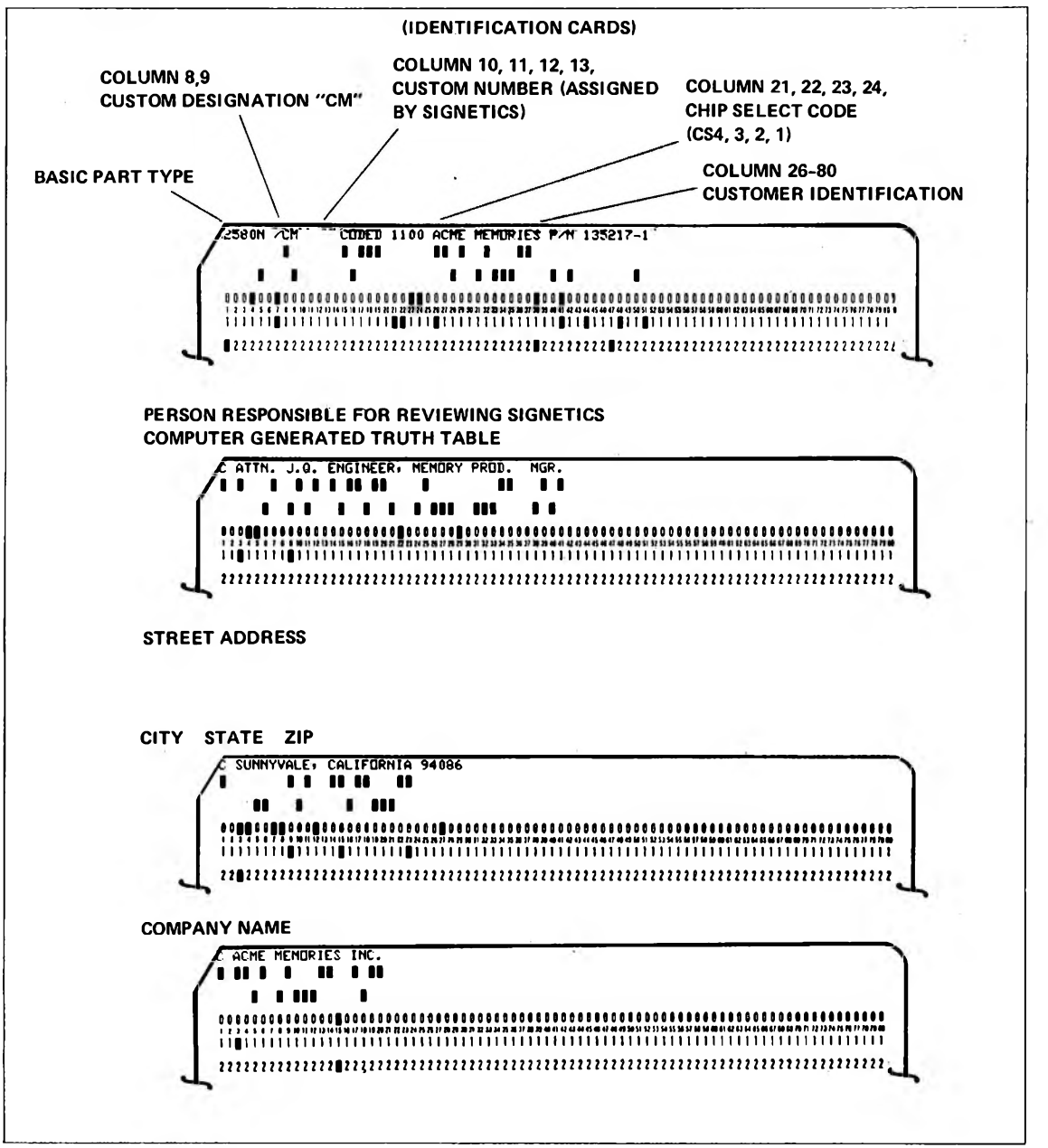


CODING FORMAT

Coding data for the 2580 may be sent to Signetics via punched cards or via a written truth table. Cards are preferred since errors are essentially eliminated.

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computor Aided Design (CAD) facility. The truth table will then be sent to the customer requesting engineer for final approval. On receipt of final approval, Signetics will cut the rubylith mask and proceed with manufacture.

CARD FORMAT



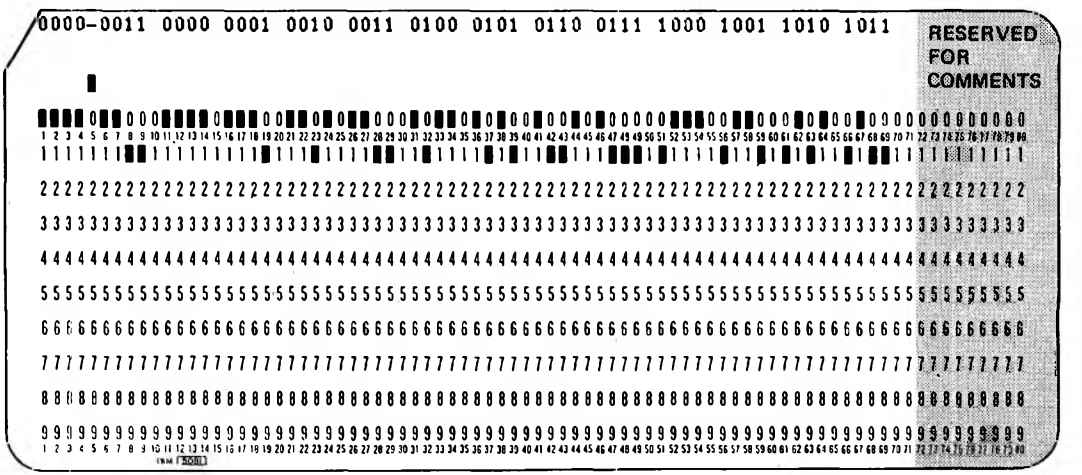
CODING FORMAT (Cont'd)

DATA CARD FORMAT

Col 1-4	Decimal equivalent of first data word location. Example: 0124 Note: leading zeros must be used for addresses from 0000 to 0999.
Col 5	Dash (-) to separate numbers
Col 6-9	Address of last data word on card
Col 10	Blank
Col 11-14	First data word (0_4, 0_3, 0_2, 0_1)
Col 15	Blank
Col 16-19	Second data word
Etc. thru column 71	
Col 72-80	Reserved for comments (These columns are ignored by the computer)

Up to twelve (12) data words can be coded on one card. Less than 12 may be used as long as the first and last addresses are given in columns 1-9.

EXAMPLE



TRUTH TABLE WORKSHEET

DECIMAL ADDRESS	O_4	O_3	O_2	O_1

DECIMAL ADDRESS	O_4	O_3	O_2	O_1

Note:
"1" = +5V
"0" = 0V
(Copy this form when submitting written truth table)