DESCRIPTION

The 25L01 employs enhancement mode p-channel MOS devices integrated on a single monolithic chip.

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics' unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide substrate structure provides an ion barrier. In addition, Signetics' proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

All inputs of the 25L01 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA, sufficient to drive one standard TTL load.

The maximum power dissipation of 1.7mW/bit is required only during read or write. For standby operation 100μW/bit is obtained by removing V_D and reducing V_{DD} to -8.0V. Removal of V_D alone wll cut power dissipation by a factor of almost 3.

The outputs of the 25L01 are effectively open circuited when the device is not selected (logic high on chip select). This feature allows OR-tying for memory expansion.

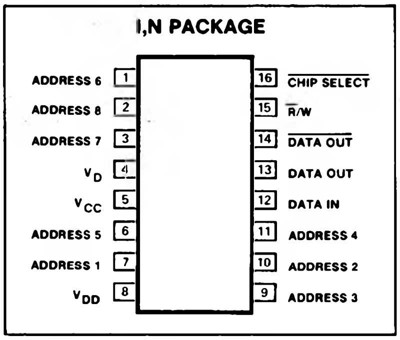
FEATURES

- **Fully decoded addresses**
- **Access time: 1.0μs guaranteed**
- **Power dissipation: 1.7mW/bit max**
- **Standby power dissipation: 100μW/bit**
- **DTL and TTL compatible**
- **Chip select and output wired-OR capability**
- **Standard 16-pin DIP**
- **P-MOS silicon gate technology**
- **Fully static**
- **Requires no clocking**
- **Optimized with +5 and -12V supplies**

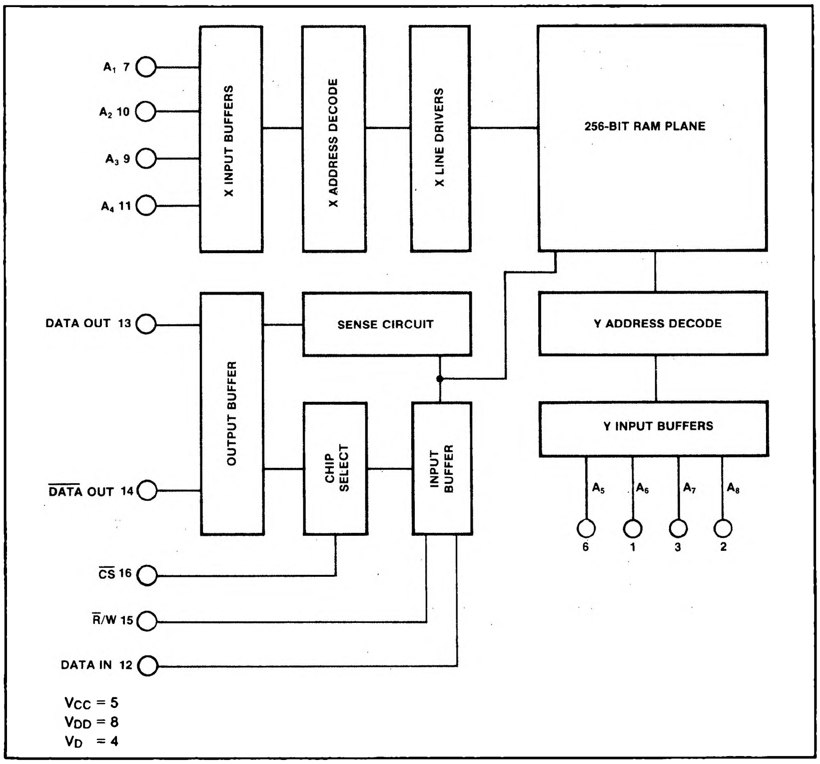
APPLICATIONS

- **Small buffer stores**
- **Small core memory replacement**
- **Bipolar compatible data storage**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to +70	
T_{STG}	Storage	-65 to +150	
P_D	Power dissipation		mW
	I package	800	
	N package	640	
	All input or output voltages with respect to the most positive supply voltage, V_{CC}	+0.3 to -20	V
	Supply voltages V_{DD} and V_D with respect to V_{CC}	-18	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{DD} = V_D = -12V ± 5% unless otherwise specified.[2,3,4,5,6,7]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low		-12		V_{CC}-4.5	
V_{IH}	High		V_{CC}-2.0		V_{CC}+0.3	
	Output voltage					V
V_{OL}	Low	I_{OL} 3.0mA		-0.7	0.45	
V_{OH}	High	I_{OH} = -100μA	3.5	4.5		
	Input current	V_{IN} = 0V, T_A = +25°C				nA
I_{LI}	Load (All input pins)			<1.0	500	
	Output current					
I_{LO}	Leakage	V_{OUT} = 0V, Chip select input = 3.3V, T_A = 25°C		<1.0	1000	nA
	Sink					
I_{OL1}		V_{OUT} = 0.45V, T_A = +25°C	3.0	6		
I_{OL2}		V_{OUT} = 0.45V, T_A = +70°C	2.0	5		
I_{OL3}		V_{OUT} = -0.7V		6	13	
	Source	V_{OUT} = 0V				mA
I_{OH1}		T_A = +25°C	-3.0	4		
I_{OH2}		T_A = +70°C	-2.0	3		
	Supply current	T_A = +25°C				mA
I_{DD}	V_{DD}			5	9	
I_D	V_D	I_{OL} = 0mA		11	16	
	Capacitance	f = 1MHz				pF
C_{IN}	Input (All pins)	V_{IH} = 5V		7	10	
C_{OUT}	Output	V_{OUT} = 5V		7	10	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ± 5%, V_{DD} = V_D = -12V ± 5%, Input pulse amplitudes = 0 to 5V, Input pulse rise and fall times = <10ns, Speed measurements referenced to 1.5V levels, Output load = 1 TTL gate, Measurements made at output of TTL gate (t_{pd} ≤ 10ns), unless otherwise specified.

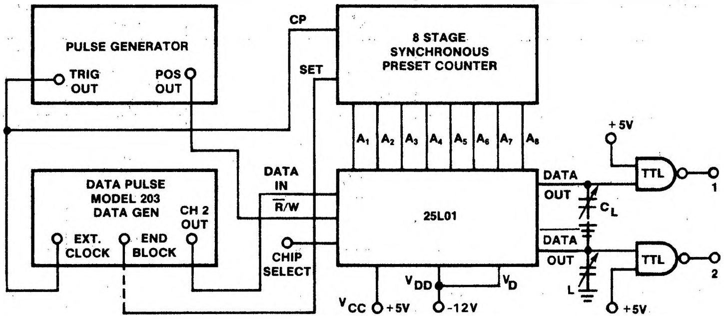
PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
READ CYCLE							
t_A	Access time	Output	Address			1000	ns
WRITE CYCLE							
t_W	Write time	Write	Address	300			ns
t_{WD}	Delay time			300			ns
t_{WP}	Write pulse width			400			ns
t_{DO}	Data-write pulse overlap			100			ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 100°C/W junction to ambient for the I package or 150°C/W for the N package.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and typical supply voltages.

TEST LOAD CIRCUIT

SPEED MEASUREMENT



NOTES

A. Each clock time is split into a Read followed by a Write. Read and Write times can be varied by adjustment of the delay and width controls of the pulse generator.

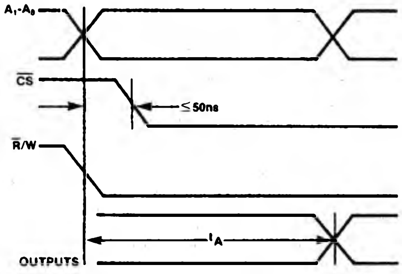
B. Data generator produces a 256-bit block of data, 32 bits repeated 8 times. PCM mode used so data can be changed in 32 bits of the 2501 from one cycle to the next.

C. All inputs to the 25L01 are standard TTL outputs with $V_{CC} = 5V \pm 5\%$.

D. Access time is measured between A1 (least significant address input) and points 1 and 2.

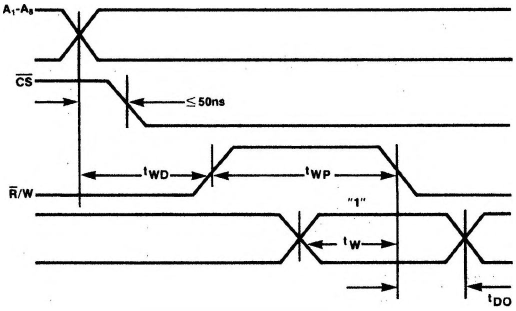
VOLTAGE WAVEFORMS

READ CYCLE



For Measurement Purpose Only

WRITE CYCLE



For Measurement Purpose Only