2600-F,I,N • 2600-1 - F,I,N

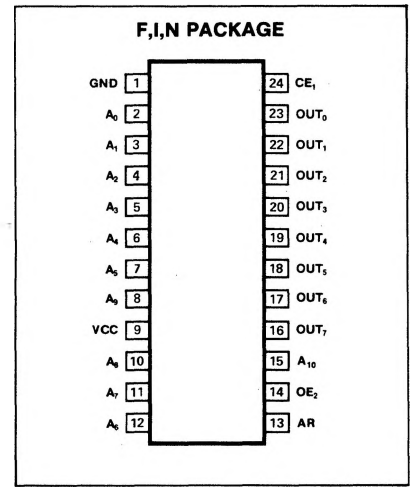
DESCRIPTION

The 2600 outputs appear and remain in a steady state condition until a new address is read. The 16,384 bits are organized as 2048 addresses with 8 output lines. Full address decoding is performed on chip. The 2600's size enhances its usage in any high density, fixed memory application such as logic function generation or microprogramming. Programming of the device is accomplished via the use of one custom mask during device fabrication.

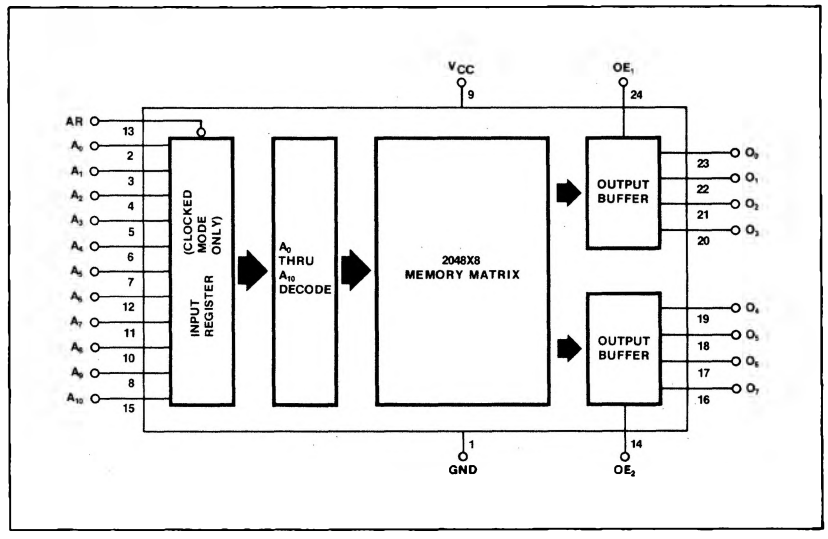
FEATURES

- **Completely static**
- **Utilizes MOS n-channel si-gate technology**
- **Clocked or unclocked operation**
- **Access time: 300/550ns max**
- **Single +5V power supply**
- **2 output enable controls allow:**
  Wire OR'D three-state outputs for expanded memories
  2048X8 or 4096X4 organization
- **All inputs and outputs directly TTL compatible**
- **Pin compatible with EA4600 and EA4900**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to +150	
P_D	Power dissipation	Hermetic 1.25	W
	Voltages on all inputs and supply pins	-0.5 to +7.0	V

ELECTRICAL DRIVE REQUIREMENTS $0°C \le T_A \le +70°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TEST CONDITIONS[2,3]	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage	Address read, address input and output enable				V
V_{IL}	Low		-0.5		0.8	
V_{IH}	High		2.2		V_{CC}	
	Output voltage	TTL interface				V
V_{OL}	Low data	I_O = 1.6mA		0.2	0.4	
V_{OH}	High data	I_O = -100μA	2.4	3.5	V_{CC}	
I_{LI}	Input leakage current	Test pin at V = V_{CC} max, Other pins at ground			10	μA
I_{CC}	Supply current	V_{CC} = V_{CC} max 25°C		80	115	mA
	Capacitance	0V bias, f = 1MHz				pF
C_{IN}	Address input			5	7.5	
C_{AR}	AR input			5	7.5	
C_{OUT}	Output			7	10	

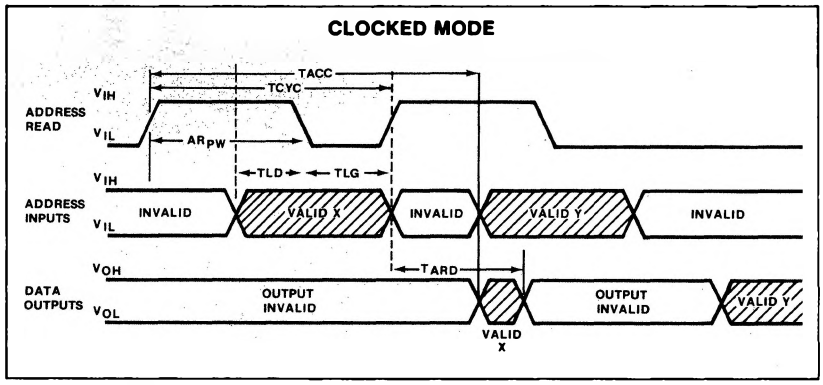
TIMING SPECIFICATIONS $0°C \le T_A \le +70°C$, $4.75V \le V_{CC} \le 5.25V$

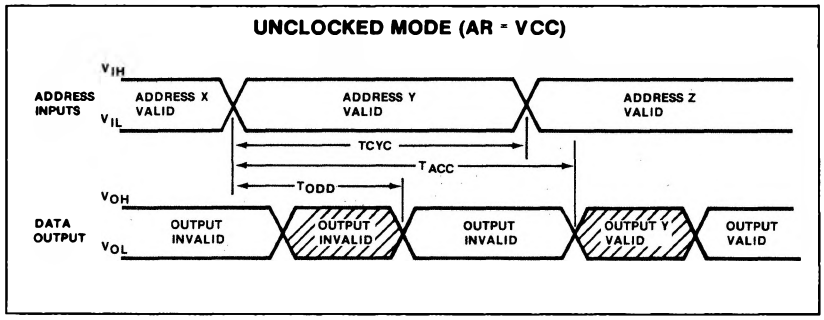
PARAMETER		TO	FROM	TEST CONDITIONS[2,3]	2600			2600-1			UNIT
					Min	Typ	Max	Min	Typ	Max	
CLOCKED MODE											
T_{CYC}	Cycle time				500			300			ns
	Pulse width										ns
AR_{PW}	Address read				300	150		100	50		
	Delay time										ns
T_{ACC}		Output	Address			450	550		200	300	
T_{ARD}		Output disturb	Address read		75	140		0	30		
T_{LD}	Address lead time				100	30		50	0		ns
T_{LG}	Address lag time				150	70		100	50		ns
UNCLOCKED MODE											
T_{CYC}	Cycle time			Standard	500			300			ns
	Delay time										ns
t_{ACC}		Output	Address			450	500		200	300	
T_{ODD}		Output disturb			0	50		0	30		
OUTPUT ENABLE (CLOCKED OR UNCLOCKED MODE)											
	Delay time										ns
T_{CO}		Output on	Output enable			100	300		(50)	150	
T_{DO}		Output off	Output enable			150	400		100	200	

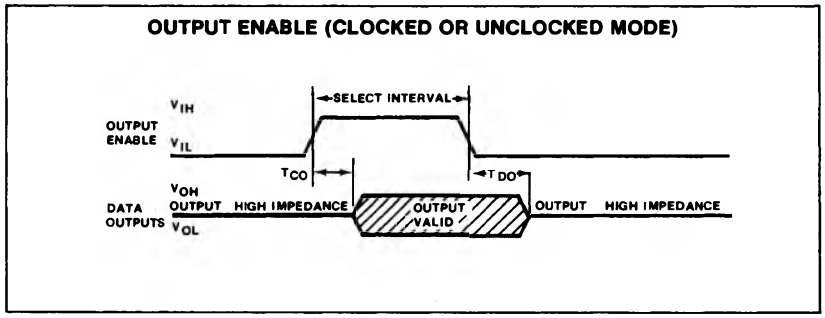
NOTES

1. Stresses more severe than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and operation of the device at any condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are referenced to V_{SS}. Positive current flows into the referenced pin.
3. Output load = 50pF plus 1 standard TTL input.

TIMING DIAGRAMS







DEFINITIONS

Clocked Mode

1. T_{CYC}, Cycle Time is the time between successive address read pulses.
2. T_{LD}, Address Lead Time is the minimum time required for the address to be valid prior to the falling edge of the AR pulse.
3. T_{LG}, Address Lag Time is the minimum amount of the time required for the address to remain valid after the falling edge of the AR pulse.
4. T_{ARD}, Address Read to Output Disturb Delay is the minimum time between the AR pulse and the first output transition when a new address is present.

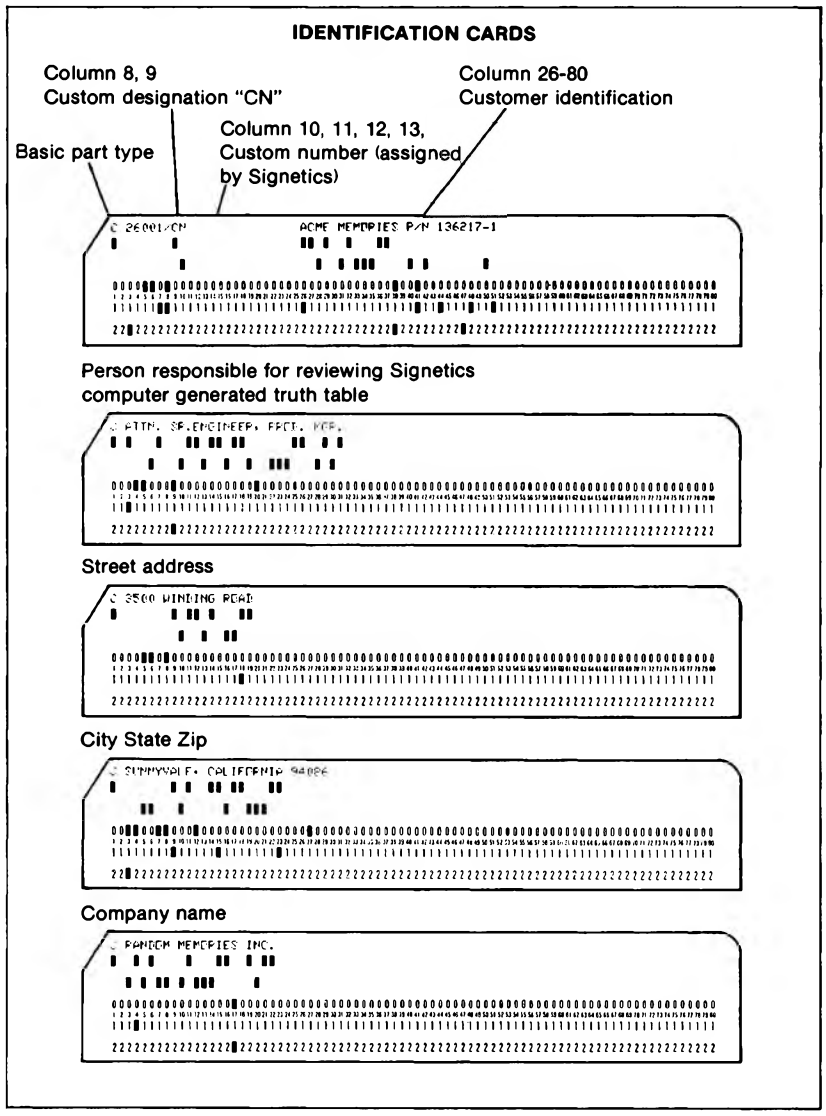
Unclocked Mode

1. T_{CYC}, Cycle Time is the time between application of successive addresses.
2. T_{ACC}, Address to Output Delay Time is the maximum time between a new valid address and the corresponding valid output.
3. T_{ODD}, Output Disturb Delay is the minimum time between the address change and the first output transition.

Output Enable

1. T_{CO}, Output Enable to Output ON Delay Time is the minimum time required for the output, in high impedance state, to become valid after rising edge of the output enable pulse.
2. T_{DO}, Output Enable to Output ON Delay Time is the minimum time required for the output to become high impedance after the falling edge of the output enable pulse.

CARD FORMAT



CUSTOM PATTERN PROGRAMMING INSTRUCTIONS

For the very large MOS ROM now produced by Signetics, a computer aided technique utilizing punched computer cards is employed. This technique requires that the customer supply Signetics with a deck of standard 80 column computer cards describing the data to be stored in the ROM array.

The required punching format is described below. All addresses must be included with their outputs defined. That is, no assumptions are made regarding the bit configuration of undefined outputs. Therefore the customer must submit cards defining the entire ROM contents, even though part or portions of the ROM may be unused (zeros).

Data Card Format for Custom ROMs

Each card is to be punched as follows. Note that for the Signetics 2600, a 3-digit octal number is used for representing the 8 ROM outputs.

Column	
1-4	Punch a 4-digit octal number representing the input address for the first of the 16 output words appearing on this card. (This is the initial address)
5-7	Punch a 3-digit octal number representing the outputs for the initial input address.
8-10	Punch a 3-digit octal number representing the outputs for the initial input address +1.
11-13	Punch a 3-digit octal number representing the outputs for the initial input address +2.
50-52	Punch a 3-digit octal number representing the outputs for the initial input address +15.
69-80	The unique number assigned to this ROM pattern by Signetics must be punched in this field enclosed by blank spaces. This number can be obtained by contacting your local Signetics salesman, representative, or the marketing department at the factory directly.

Each card, therefore, carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the unique ROM number. The card must be provided for all possible sequential address locations (in blocks of 16). A 2048 word ROM, therefore, requires 128 cards, with all 16 output words defined on each card.