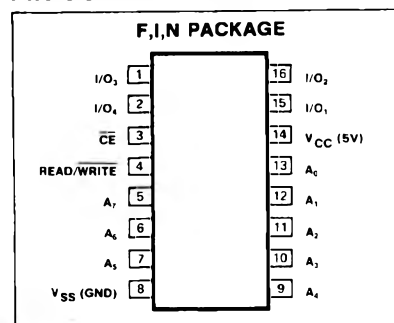
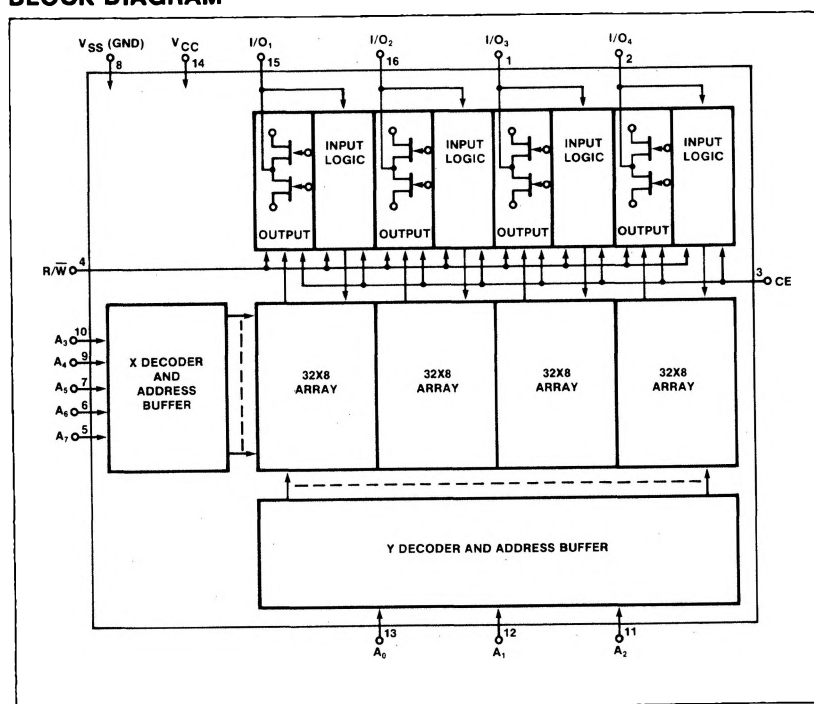


DESCRIPTION

The 2606 is fabricated with n-channel silicon gate MOS technology and achieves an access time of less than 750ns.

FEATURES

- Fully decoded
- No clocks required
- All interface signals, including power supply directly TTL compatible

PIN CONFIGURATION**BLOCK DIAGRAM****ABSOLUTE MAXIMUM RATINGS¹**

PARAMETER	RATING	UNIT
T_A	Temperature range	$^{\circ}\text{C}$
T_{STG}	Operating under bias	0 to 70
	Storage	-65 to 150
P_D	Power dissipation	1
	Voltage on any pin with respect to ground	-0.5 to 7
		W
		V

DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ²	Max	
V_{IL} V_{IH}	Input voltage Low High	-0.5 2.2		0.65 V_{CC}	V
V_{OL} V_{OH}	Output voltage Low High			0.45	V
		$I_{OL} = 1.9\text{mA}$ $I_{OH} = -100\mu\text{A}$			
		2.4			
I_{LI}	Input current	$V_{IN} = 0$ to 5.25V			μA
I_{LOH} I_{LOL}	I/O leakage current	$\overline{CE} = 2.2\text{V}$ $V_{I/O} = 4.0\text{V}$ $V_{I/O} = 0.45\text{V}$			μA
					10
I_{CC1} I_{CC2}	Supply current	$V_{IN} = 5.25\text{V}$, $I_{I/O} = 0\text{mA}$ $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$			mA
					70 80
C_{IN} $C_{I/O}$	Capacitance ³ Input (All pins) I/O	$T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$ $V_{IN} = 0\text{V}$ $V_{OUT} = 0\text{V}$			pF
					4 7 10

AC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$ unless other specified.^{4,5,6,7}

PARAMETER	TO	FROM	2606			2606-1			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_R t_A T_{RO}^8 t_{CO}^8	Output enable Output enable	Read Chip enable	750		750	500		500	ns ns ns ns
			100			75			
			0			0			
						0			
t_{VC} t_{VA}	Previous data valid with respect to Chip disable Address change		0 50		150	0 50		100	ns
t_{CV} t_{RC}	Delay time	Data valid Chip enable	100		400	50		300	ns ns
t_W t_{AW} t_{WW} t_{WR}	WRITE CYCLE A Write cycle time Write pulse width Write recovery time	Write Address	750 250 400 100			500 150 300 50			ns ns ns ns
t_{CS} t_{CH}	Setup and hold time Setup time Hold time	R/W Chip enable	0			0			ns
t_{DS} t_{DH}	Setup time Hold time ⁹	R/W Data	380 0			280 0			
t_{WD}	Disable delay ¹⁰	Data out			125			100	ns
t_W t_{AC} t_{CW} t_{CR}	WRITE CYCLE B Write cycle time Chip enable pulse width Chip enable recovery time	Chip enable Address	750 250 400 100			500 150 300 50			ns ns ns ns
t_{WS} t_{WH}	Setup and hold time ¹¹ Setup time Hold time	Chip enable R/W	200 0			100 0			ns
t_{DS} t_{DH}	Setup time Hold time ⁹	Chip enable Data	380 0			280 0			

NOTES on following page.

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for $T_A = 25^\circ\text{C}$ and typical supply voltage.
3. This parameter is periodically sampled and is not 100% tested.
4. Input levels swing between 0.65V and 2.2V.
5. Input signal transition times are 20ns.
6. Timing reference level is 1.5V.
7. Bus load is 100pF, 1 TTL tri-state output.
8. R/W must be high and CE must be low in order for output buffers to turn on.
9. Maximum t_{DH} governed by potential conflict with data out during next cycle.
10. The output buffers will turn off within the specified time after write mode is selected.
11. Write setup required to prevent data overlap. For write cycle B the R/W line will typically change with the addresses.

TIMING DIAGRAM

