DESCRIPTION

The Signetics 2655 PPI is designed for 2650 microcomputer systems. It consists of three ports (24 I/O pins), which can be individually programmed to function as input, output or bidirectional ports. Interface with the 2650 is via an eight-bit bidirectional data bus.

The PPI may be programmed for five major modes of operation: static I/O, strobed I/O, bidirectional I/O, serial I/O, or serial/timer I/O. In the serial/timer mode, parallel to serial or serial to parallel conversion of data operates simultaneously with the timer on one of the three ports.

FEATURES

- **Five selectable major operating modes:**
  - **Static I/O**
  - **Strobed I/O**
  - **Bidirectional**
  - **Serial I/O**
  - **Serial/timer I/O**
- **Three ports (A, B, and C) with 24 programmable I/O pins**
- **Completely TTL compatible**
- **Three MHz programmable timer or event counter**
- **Fully compatible with the 2650 microprocessor**
- **Direct bit set/reset capability of each bit for all three ports**
- **300ns port read/write access time**
- **Operates in a polled or interrupt driven system environment**
- **Forty pin dual in-line package**
- **Single +5 volt supply**

OPERATION

The following is a functional description of the five operating modes of the PPI. Each mode is selected via a mode control word. Interrupt generation and interrupt enable/disable functions are available with each mode except the static mode which operates entirely under program control.

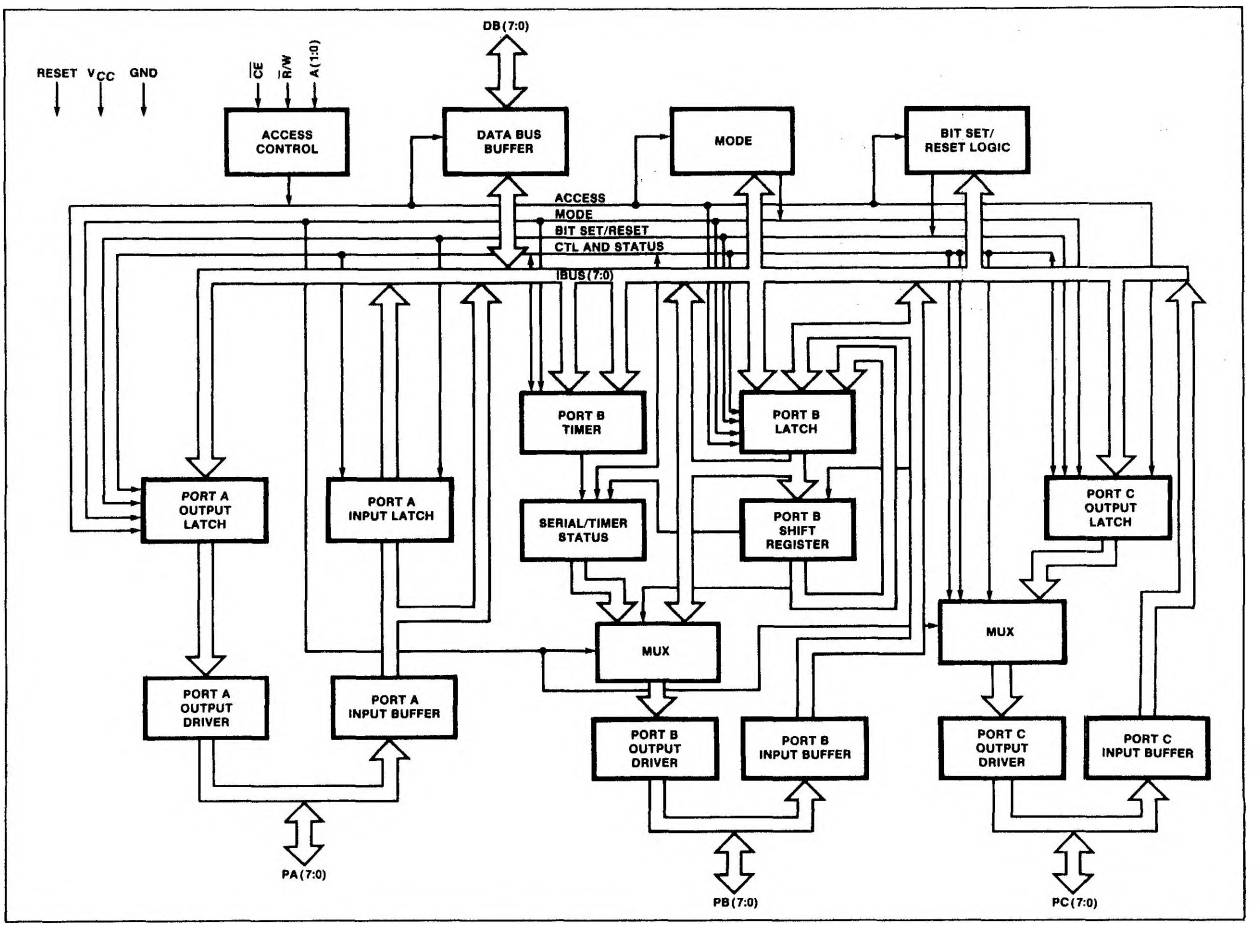
STATIC MODE

All three ports can operate in the static I/O mode. This mode allows each pin of each port to be either an input pin or an output pin. A logic "1" written to a pin of a selected port from the 2650 will condition that pin to be an input or output pin. Writing a logic "0" to the pin conditions that pin to be an output pin only. Outputs are latched while inputs are not. Each pin may be set or reset on an individual basis by a "set/reset" command.

STROBED I/O MODE

In this mode, data may be transferred to or from a specified port in conjunction with strobe or "handshaking" signals. Ports A and B can operate in the strobed I/O mode and port C bits are used as control and status bits. In this mode both inputs and outputs are latched, and each port can be either an input or output.

BLOCK DIAGRAM



BIDIRECTIONAL I/O MODE

This mode provides a means for communicating with a peripheral device over a single eight-bit bus with both transmitting and receiving capability. Port A operates in this mode with Port C pins providing "handshaking" signals for status and control. Both inputs and outputs are latched and port direction is determined by a control signal from the peripheral.

SERIAL I/O MODE

This mode provides a means for communicating with a peripheral device on a bit serial basis through Port B. Parallel data from the CPU will be shifted out to the peripheral over the least significant bit of Port B (PB0). Eight clocks will be required for a complete character transfer. The eight-bit character will be repeatedly shifted out until the CPU presents another character to Port B.

For the serial in mode, data is input from the peripheral at the most significant bit of Port B (PB7). Eight clocks will be required to assemble the eight-bit character. An interrupt request will signal the CPU for character transfer.

TIMER MODE

This mode enables the PPI to perform time interval measurements, pulse width measurements, and event counting. This timing function is performed during the serial/timer mode, and is restricted to Port B only. The mode is initiated by selecting the desired operation and loading a 16-bit down counter with an initial value. The counter does not start counting until the upper eight bits have been loaded. An interrupt can be generated to signal the CPU when the timer reaches a zero count.

PIN DESIGNATION

PIN NO.	MNEMONIC	TYPE	NAME AND FUNCTION
27-34	D7-D0	I/O	**Data Bus:** Eight-bit tri-state bidirectional data bus. All data and command transfers are made using this bus. D0 is the least-significant bit; D7 is the most-significant bit.
35	RESET	I	**Reset:** Resets all internal storage elements, including the data latches and command registers. Resets ports A, B and C to accept input data, and operating mode to Static mode. A functionally equivalent on chip power-on reset is also provided.
8,9	A1, A0	I	**Address:** Address lines used to select internal PPI modes or registers. Indicates control or data words to be placed on the data bus. Used in conjunction with the $\overline{R}$/W line.
5	$\overline{R}$/W	I	**Read/Write:** When low, gates the selected register to the data bus. When high, gates the contents of the data bus into the selected register.
6	$\overline{CE}$	I	**Chip Enable:** When low, identifies that control and data lines to the PPI are valid.
36	$\overline{SCLK}$	I	**Serial Clock:** Provides a serial clock for the parallel-to-serial or serial-to-parallel conversion.
37-40 1-4	I/O PA7-PA0	I/O	**Port A:** An eight-bit tri-state quasi-bidirectional port.* PA0 is the least-significant bit; PA7 is the most-significant bit.
25-18	I/O PB7-PB0	I/O	**Port B:** An eight-bit quasi-bidirectional port.* PB0 is the least-significant bit; PB7 is the most-significant bit. Port B also has parallel-to-serial, or serial-to-parallel conversion capability with PB0, 7 being either the serial output or input respectively. Data is double buffered. Port B can also operate as a 16-bit binary timer, as an event counter, or as a pulse width indicator. An output is generated whenever the counter is decremented to the all-zero state.
10-13 17-14	I/O PC7-PC0	I/O	**Port C:** An eight-bit quasi-bidirectional port.* PC0 is the least-significant bit; PC7 is the most significant bit. Port C bits are also used as control and status signals in conjunction with ports A and B. When a pin is used as a strobe input, the line receives an external strobe input which clocks information from port A or port B into the port A or port B data latches. When a pin is used as a status line, the line indicates port A or port B status condition which may be used as an interrupt input to the 2650.
26		I	**+5 Volt:** Power supply.
7		I	**Ground:** 0V reference.

*A quasi-bidirectional port allows each bit to be designated as input or output under program control. If any bit of the port is set to a '1,' that bit becomes an input or output depending on the usage of the port pin. If the peripheral is driving the port bit (i.e., overriding the logic "1" condition produced by the internal port pull up resistor), then the bit is an input. If the peripheral is receiving from the port bit, then a "0" or "1" written to the port will be transmitted to the peripheral.