DESCRIPTION

The 4-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPUs, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the 2901-1 will allow efficient emulation of almost any digital computing machine.

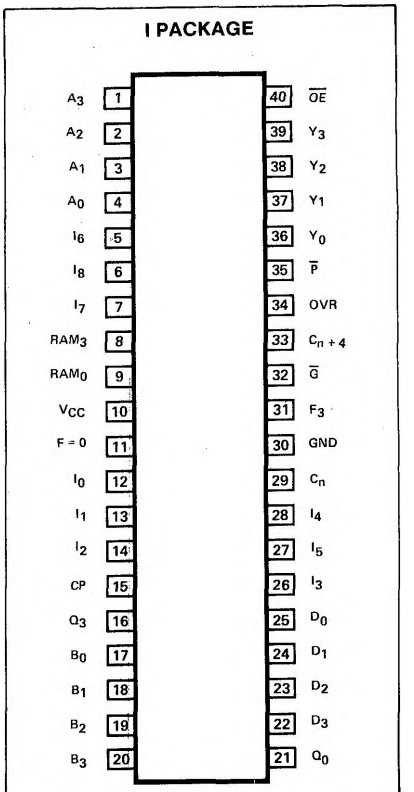
The device, as shown in the block diagram below, consists of a 16-word by 4-bit 2-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The 9-bit microinstruction word is organized into 3 groups of 3 bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

FEATURES

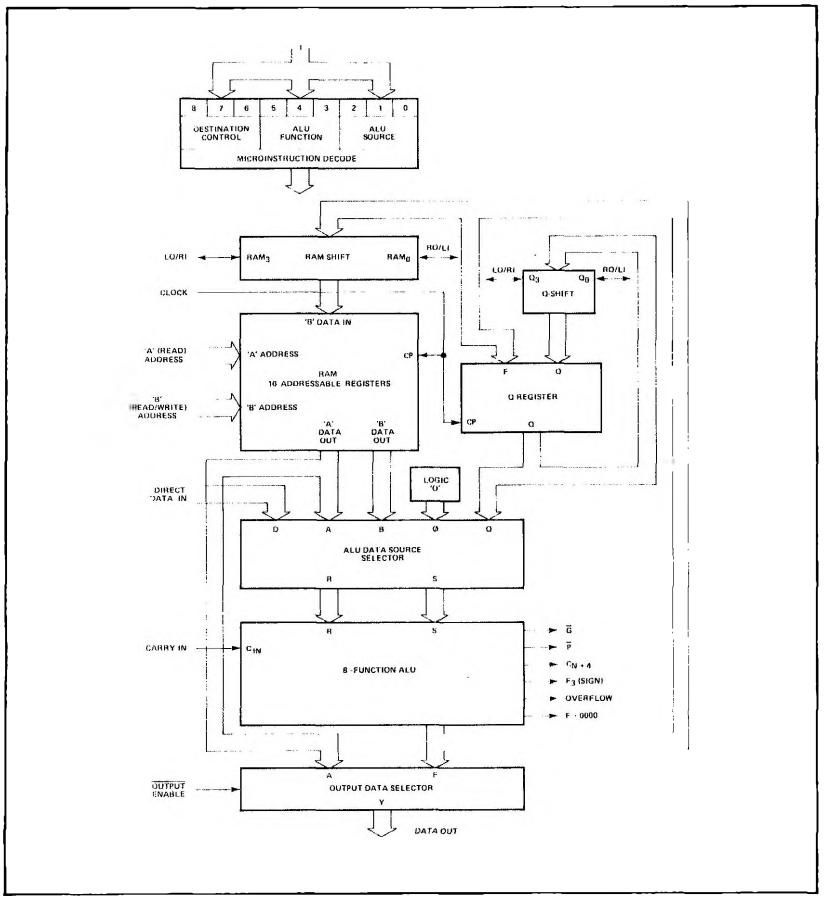
- **80ns cycle time**
- **2-address architecture**
  Independent simultaneous access to 2 working registers saves machine cycles
- **8-function ALU**
  Performs addition, 2 subtraction operations, and 5 logic functions on 2 source operands
- **Flexible data source selection**
  ALU data is selected from 5 source ports for a total of 203 source operand pairs for every ALU function
- **Left/right shift independent of ALU**
  Add and shift operations take only 1 cycle
- **4 status flags**
  Carry, overflow, zero, and negative
- **Expandable**
  Connect any number of 2901-1's together for longer word lengths
- **Microprogrammable**
  3 groups of 3 bits each for source operand, ALU function, and destination control

PIN CONFIGURATION

I PACKAGE



BLOCK DIAGRAM



PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-4	A_0-A_3	**A Address** The 4 address inputs to the register stack used to select 1 register whose contents are displayed through the A port. A_0 is the LSB.	Active high
17-20	B_0-B_3	**B Address** The 4 address inputs to the register stack used to select 1 register whose contents are displayed through the B port and into which new data can be written when the clock goes LOW. B_0 is the LSB.	Active high
12-14, 26-28, 5-7	I_0-I_8	**Instruction Control** The 9 instruction control lines to the 2901-1 used to determined what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q register or the register stack (I_{678}).	Active high
8 16	RAM_3 Q_3	**Shift Line** A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the 2901-1. When the destination code on I_{678} indicates a left (up) shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are off (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a right (down) shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).	Three-state Active high
9 21	RAM_0 Q_0	**Shift Line** Shift lines similar to Q_3 and RAM_3, at the LSB of the Q register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device and are used to transfer data between devices for left and right shifts of the Q register and ALU data.	Active high
22-25	D_0-D_3	**Direct Data Inputs** A 4-bit data field which may be selected as one of the ALU data sources for entering data into the 2901-1. D_0 is the LSB.	Active high
36-39	Y_0-Y_3	**Data Out** The 4 data outputs of the 2901-1. These are three-state output lines. When enabled, they display either the 4 outputs of the ALU or the data on the A port of the register stack, as determined by the destination code I_{678}. Y_0 is the LSB.	Three-state Active high
40	$\overline{OE}$	**Output Enable** When $\overline{OE}$ is High, the Y outputs are disabled; when $\overline{OE}$ is Low, the Y outputs are active (high or low).	Active low
32, 35	$\overline{G}$, $\overline{P}$	**Carry Generate, Propagate** The carry generate and propagate outputs of the 2901-1. These signals are used with the N74S182 for carry-lookahead. See Table 7 for the logic equations.	Active low
34	OVR	**Overflow** This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit. See Table 7 for logic equation.	Active high
11	F = 0	**F = 0** This is an open collector output which goes High (off) if the data on the 4 ALU outputs F_{0-3} are all low. In positive logic, it indicates the result of an ALU operation is zero.	Active high
29	C_n	**Carry In**	Active high
33	C_{n+4}	**Carry Out** (See Table 7 for logic equations.)	Active high
15	CP	**Clock** The Q register and register stack outputs change on the clock Low-to-High transition. The clock Low time is internally the write enable to the 16X4 RAM which comprises the "master" latches of the register stack. While the clock is Low, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.	Active high

SYSTEM DESCRIPTION

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a 4-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are 4 bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A port and B port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This 3-input multiplexer scheme allows the data to be shifted up (left) 1 bit position, shifted down (right) 1 bit position, or not shifted in either direction.

The RAM A port data outputs and RAM B port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is low. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform 3 binary arithmetic and 5 logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A port and the direct data inputs (D) connected as inputs. Likewise, the ALU S input multiplexer has the RAM A port, the RAM B port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These 5 inputs, when taken 2 at a time, result in 10 possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only 7 completely non-redundant source operand pairs for the ALU. The 2901-1 microprocessor implements 8 of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the 8 source operand combinations are as shown in Table 1. Also shown is the octal code for each selection.

DETAILED 2901-1 BLOCK DIAGRAM

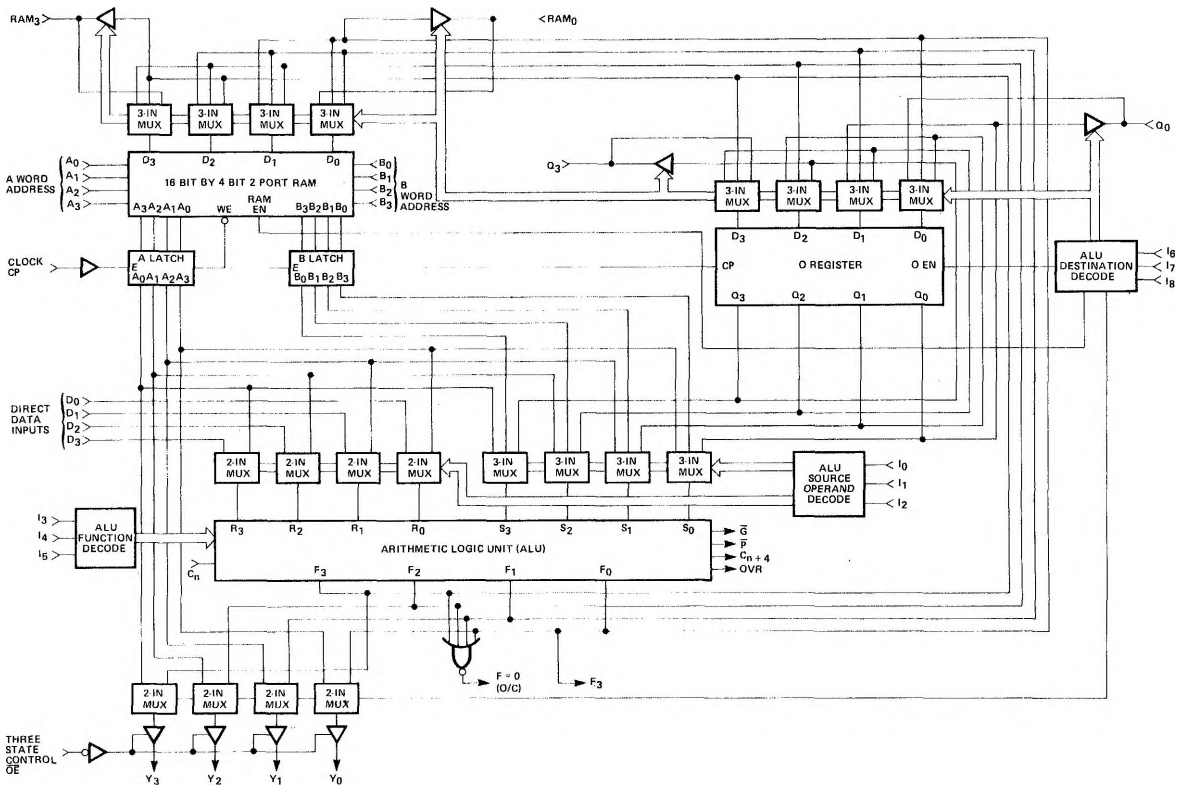


Figure 1

MICRO CODE				ALU SOURCE OPERANDS	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	0	Q
L	H	H	3	0	B
H	L	L	4	0	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	0

Table 1 ALU SOURCE OPERAND CONTROL

The 2 source operands not fully described as yet are the D input and Q input. The D input is the 4-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing 3 binary arithmetic and 5 logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Table 2. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, G, and carry propagate, P, are outputs of the device for use with a carry-look-ahead-generator such as the N74S182. A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active high.

MICRO CODE			ALU	
I_5	I_4	I_3	Octal Code	Function	Symbol
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S - R
L	H	L	2	R Minus S	R - S
L	H	H	3	R OR S	$R \vee S$
H	L	L	4	R AND S	$R \wedge S$
H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
H	H	L	6	R EX-OR S	$R \forall S$
H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Table 2 ALU FUNCTION CONTROL

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is high when all F outputs are low. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is high when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstructon inputs. These combinations are shown in Table 3.

The 4-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is high, the Y outputs are in the high-impedance state.

A 2-input multiplexer is also used at the data output such that either the A port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Table 3 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a 3-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up (left) one position (X2) or shifted down (right) one position (÷2). The shifter has 2 ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7, and I_8 microinstruction inputs as defined in Table 3.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has 2 ports; one is labeled Q_0 and the other is Q_3. The operation of these 2 ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Table 3.

The clock input to the 2901-1 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the low-to-high transition of the clock. When the clock input is high, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is low, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is low.

MICRO CODE				RAM FUNCTION		Q REGISTER FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0 LO/RI	RAM_3 LI/RO	Q_0 LO/RI	Q_3 LI/RO
L	L	L	0	X	None	None	F → Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F → B	X	None	A	X	X	X	X
L	H	H	3	None	F → B	X	None	F	X	X	X	X
H	L	L	4	Right (Down)	F/2 → B	Right (Down)	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	Right (Down)	F/2 → B	X	None	F	F_0	IN_3	Q_0	X
H	H	L	6	Left (Up)	2F → B	Left (Up)	2Q → Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	Left (Up)	2F → B	X	None	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.

Table 3 ALU DESTINATION CONTROL

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Table 4 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Table 5 defines the various logic operations that the 2901-1 can perform and Table 6 shows the arithmetic functions of the device. Both carry-in low (C_n = 0) and carry-in high (C_n = 1) are defined in these operations.

OCTAL I_{543}, I_{210}	GROUP	FUNCTION
4 0	AND	A ∧ Q
4 1		A ∧ B
4 5		D ∧ A
4 6		D ∧ Q
3 0	OR	A ∨ Q
3 1		A ∨ B
3 5		D ∨ A
3 6		D ∨ Q
6 0	EX-OR	A ∀ Q
6 1		A ∀ B
6 5		D ∀ A
6 6		D ∀ Q
7 0	EX-NOR	$\overline{A \forall Q}$
7 1		$\overline{A \forall B}$
7 5		$\overline{D \forall A}$
7 6		$\overline{D \forall Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$ ∧ Q
5 1		$\overline{A}$ ∧ B
5 5		$\overline{D}$ ∧ A
5 6		$\overline{D}$ ∧ Q

Table 5 ALU LOGIC MODE FUNCTIONS (C_n Irrelevant)

OCTAL I_5 I_4 I_3 / I_{210} OCTAL	ALU Source / ALU Function	0	1	2	3	4	5	6	7
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
	C_n = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C_n = L S Minus R	Q-A-1	B-A-1	Q-1	B-1	A-1	A-D-1	Q-D-1	-D-1
	C_n = H	Q-A	B-A	Q	B	A	A-D	Q-D	-D
2	C_n = L R Minus S	A-Q-1	A-B-1	-Q-1	-B-1	-A-1	D-A-1	D-Q-1	D-1
	C_n = H	A-Q	A-B	-Q	-B	-A	D-A	D-Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus; - = Minus, ∨ = OR; ∧ = AND, ∀ = EX-OR

Table 4 SOURCE OPERAND AND ALU FUNCTION MATRIX

OCTAL	C_n = 0 (LOW)		C_n = 1 (HIGH)	
I_{543}, I_{210}	Group	Function	Group	Function
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

Table 6 ALU ARITHMETIC MODE FUNCTIONS

LOGIC FUNCTIONS FOR $\overline{G}$, $\overline{P}$, C_{n+4}, AND OVR

The four signals $\overline{G}$, $\overline{P}$, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the 2901-1 is in the add or subtract mode. Table 7 indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Table 1.

I_{543}	FUNCTION	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S - R	← Same as R+S equations, but substitute $\overline{R}_i$ for R_i in definitions →			
2	R - S	← Same as R+S equations, but substitute $\overline{S}_i$ for S_i in definitions →			
3-7	All logic operations	High	Low	High	High

Table 7 LOGIC EQUATIONS

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

DC ELECTRICAL CHARACTERISTICS $0°C \leq +70°C$, 4.75V, $V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OH}	High level output voltage	V_{CC} = 4.75V, I_{OH} = 1.6mA	2.4			V
I_{CEX}	Output leakage current for F = 0 output	V_{CC} = 4.75V, V_{OH} = 5.25V, $V_{IN} = V_{IH}$ or V_{IL}			250	μA
V_{OL}	Low level output voltage	V_{CC} = 4.75V				
	Y	I_{OL} = 20mA			0.5	V
	$\overline{G}$	I_{OL} = 16mA			0.5	V
	C_{n+4}, F = 0, OVR, $\overline{P}$, F_3	I_{OL} = 10mA			0.5	V
	$RAM_{3,0}$, $Q_{3,0}$	I_{OL} = 6mA			0.5	V
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_I = -18mA			-1.5	V
I_I	High level input current at maximum input voltage	V_{CC} = 5.25V, V_I = 5.5V			1.0	mA
I_{IH}	High level input current	V_{CC} = 5.25V, V_I = 2.7V				
	Clock, $\overline{OE}$, A, B, D, I, C_n				20	μA
	$RAM_{3,0}$, $Q_{3,0}$ (Note 1)				20	μA
I_{IL}	Low level input current	V_{CC} = 5.25V, V_I = 0.5V				
	Clock, DE, A, B, D, I, C_n				50	μA
	$RAM_{3,0}$, $Q_{3,0}$ (Note 1)				-100	μA
I_{OS}	Short circuit output current (Note 2)	V_{CC} = 5.25V	-10		-40	mA
I_{OZ}	High-Z state output current $Y_0 - Y_3$	V_0 = 2.4V			50	μA
		V_0 = 0.5V			-50	μA
	$RAM_{3,0}$, $Q_{3,0}$	V_0 = 2.4V			100	μA
		V_0 = 0.5V			-100	μA
I_{CC}	Supply current	V_{CC} = 5.25V		165	265	mA

NOTES

1. LO/RI and RO/LI are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{676} in a state such that the three-state output is OFF.
2. Not more than 1 output should be shorted at a time. Duration of the short-circuit test should not exceed 1 second.

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
T_A	Operating temperature range	0° to +70°	°C
T_{STG}	Storage temperature range	-65° to +150°C	°C

AC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%

	PARAMETER	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Clock Times[1]				
t_{CY}	Clock cycle time	80	65		ns
t_{RMW}	Ready-modify-write cycle	70	55		ns
f_Q	Clock frequency to shift Q register	25	30		MHz
t_{CL}	Clock low period	30	22		ns
t_{CH}	Clock high period	30	13		ns
	Hold Times[1]				
t_H	Any input	0	-3		ns
	Setup Times[1]				
t_{SAB}	A, B, setup time[2, 3, 4]	90	65		ns
		t_{CL} + 30	t_{CL} + 15		ns
t_{SBD}	B destination setup time[2, 3, 4]	t_{CL} + 15	t_{CL} + 5		ns
t_{SD}	D input setup time	60	45		ns
t_{SCn}	Cn input setup time	50	35		ns
t_{SI012}	ALU source control setup time	80	60		ns
t_{SI345}	ALU function setup time	75	58		ns
t_{SI678}	ALU destination control setup time[5]	t_{CL} + 25	t_{CL}+15		ns
t_{SS}	$RAM_{3,0}$, input setup time	30	20		ns
	$Q_{3,0}$	15	10		

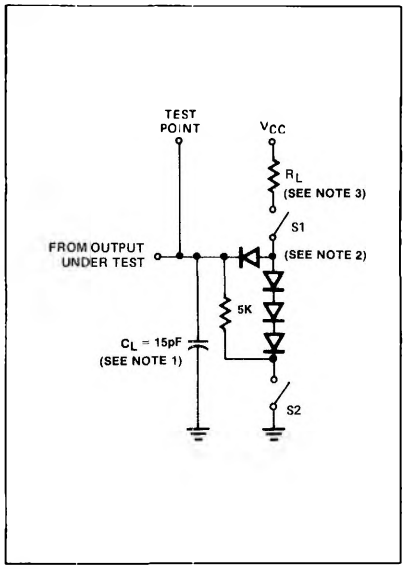
NOTES

1. Setup and hold times are defined relative to the clock low-to-high edge. Inputs must be steady at all times from the setup time prior to the clock until the hold after the clock. The setup times allow sufficient time to perform the correct operation on the correct operation on the correct data so that the correct ALU data can be written into one of the registers.
2. If the B address is used as a source operand, allow for the A, B source setup time; if it is used only for the destination address, use the B dest. setup time.
3. Where 2 numbers are shown, both must be met
4. t_{CL} is the clock low time

PROPAGATION DELAYS (ns) C_L = 15pF T_A = 0° to +70°C, V_{CC} = 5.0V ± 5%

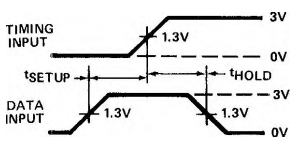
From Input \ To Output	Y	F_3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0 RL = 470	OVR	SHIFT OUTPUTS	
							RAM	Q
Clock	60	55	45	50	65	50	65	45
A, B	75	65	60	70	80	60	80	—
D (arithmetic mode)	40	30	30	40	55	40	55	—
D(I = X37, logic mode)	40	30	—	--	55	—	55	—
C_n	40	25	25	—	45	30	50	—
I_{012}	60	50	45	50	60	45	65	—
I_{345}	55	40	40	50	50	45	60	—
I_{678}	30	—	—	—	—	—	45	45
$\overline{OE}$ Enable/Disable	25/30	—	—	—	—	—	—	—
A bypassing ALU (I = 2xx)	45	—	—	--	—	—	—	—

TEST LOAD CIRCUIT

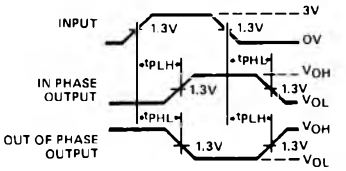


VOLTAGE WAVEFORMS

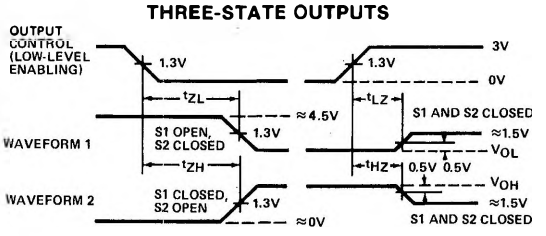
SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES THREE-STATE OUTPUTS

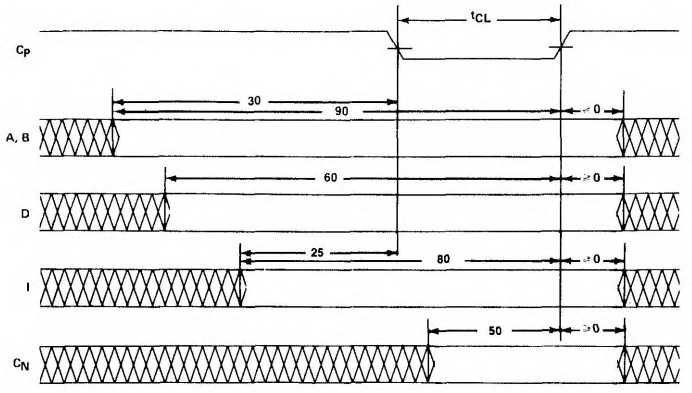


NOTES

1. C_L includes probe and jig capacitance.
2. All diodes 1N916 or 1N3064.
3. R_L = 2K

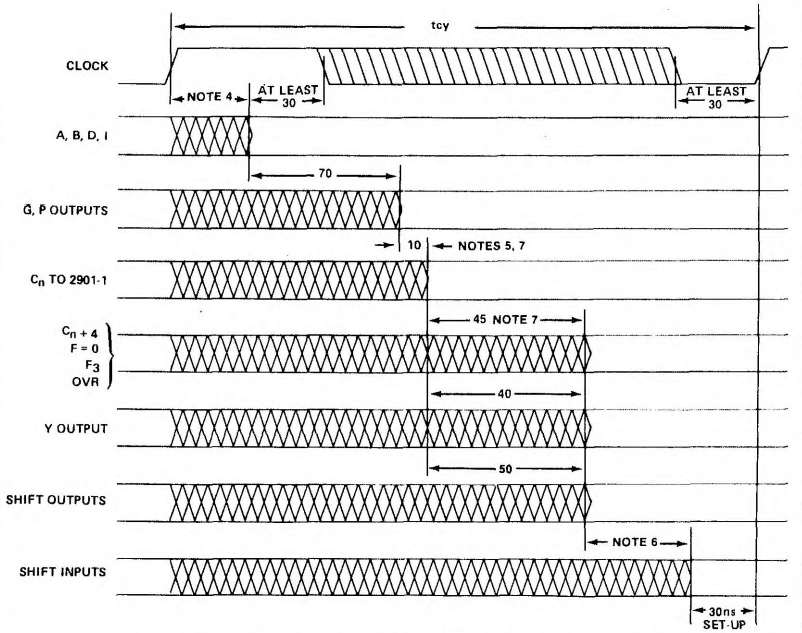
VOLTAGE WAVEFORMS (Cont'd) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

MINIMUM CYCLE TIMES FROM INPUTS



Numbers Shown Are Minimum Data Stable Times for 2901-1, DC, in ns.

SWITCHING WAVEFORMS FOR 16-BIT SYSTEM



Assuming A, B, D, and I are all Driven from Registers with the same Propagation Delay, Clocked by the 2901-1 Clock.

NOTES

4. This delay is the max. tpd of the register containing A, B, D, and I.
5. 10ns for lookahead carry. For ripple carry over 16 bits use 2 x (Cn → Cn + 4).
6. This is the delay associated with the multiplexer between the shift outputs and shift inputs on the 2901-1s. Normally applicable only for double length or circular shifts.
7. Not applicable for logic operations.