29C84A*

Digital to Analog Video Decoder

Description

New video transmission systems like D2-MAC/packet and ISDN are being introduced today. These new services are using digital coding and decoding of video signals. The 29C84A is a digital to analog video processor intended for conversion of composite input signals into analog red, green and blue signals. It fully complies with the new MAC video specifications and CCIR 601 recommendation. The digital inputs are coded on 8 bits, the luminance (Y) is sampled at 13.5 MHz and the multiplexed chrominance (CR, CB) is sampled at 6.75 MHz. This sampling frequency is equivalent to 702 points per active line in 625-line television systems.

The 29C84A is processed in an advanced 1 µm analog CMOS technology, it is composed of a filtering stage for elimination of the duplicated spectra introduced by digitization, a dematrixing stage and three D to A converters delivering the R, G, B signals.

High frequency operation (27 MHz) is possible because of parallel architecture and the 29C84A can be used for a wide range of applications including still picture transmission at n × 64kbps (ISDN), video conference and D2-MAC satellite receivers.

The digital RGB bus can be used as direct inputs to the Triple DAC's.

Conversely, the outputs from the filter can be monitored on the RGB bus, under a different mode of operation.

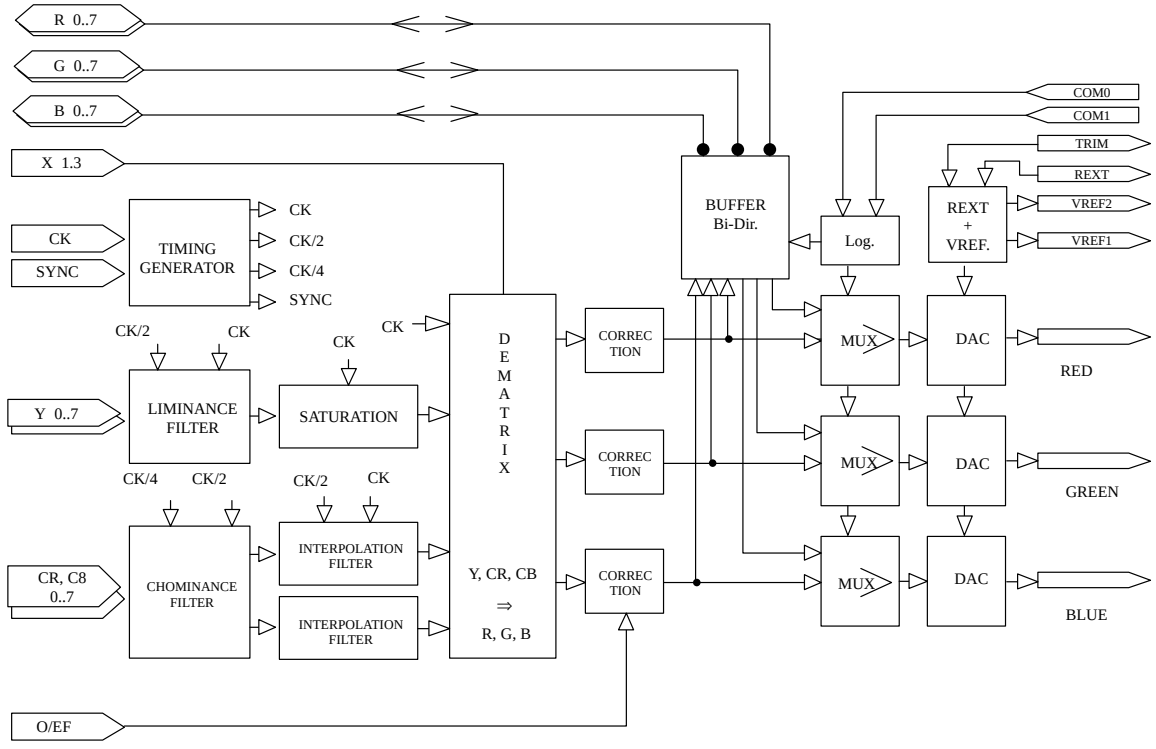
Features

- Y, CR, CB, to R, G, B decoder
- Digital to analog converters for R, G, B
- Elimination of duplicated spectra by oversampling
- 7th Order chrominance filter with programmable cutoff (1, 1.3, 1.6 and 2MHz)
- 19th order luminance filter
- Compatibility with CCIR 601 recommendation and MAC standard
- External R, G, B digital to analog conversion capability (TV picture and alphanumeric characters mixing capability)
- Blanking level drive capability (16)
- Programmable . 75 compensation factor for D2-MAC standard
- Frame interleave capability
- Maximum operating frequency = 27MHz
- 75 Ohms/20pF load capability for DAC's
- Single 5V supply
- 1 µm analog CMOS technology
- Package : PLCC68

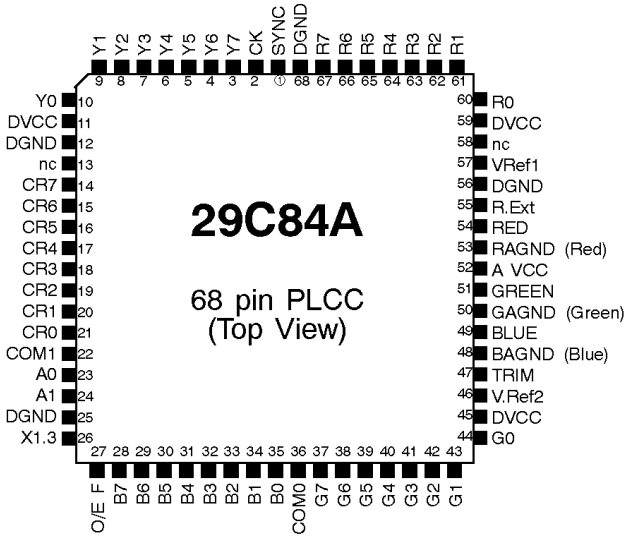
* 29C84 is under CNET licence.

Interface

Block Diagram



Pin Configuration



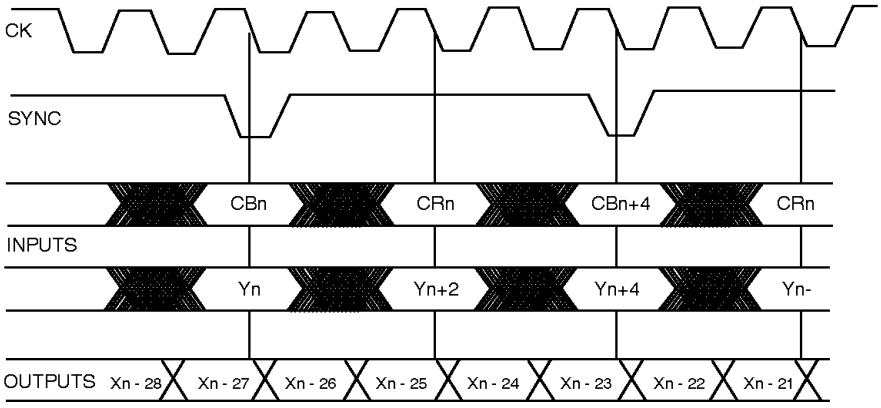
Pin Description

Pin No	Name	Function	Direction
1	SYNC	CR, CB VALIDATION CLOCK	I
2	C K	SYSTEM CLOCK (27MHz)	I
3..10	Y[7..0]	LUMINANCE	I
14..21	CR[7...0]	MULTIPLEXED CHROMINANCE CR, CB	I
12, 25, 56, 68	DGND	DIGITAL GROUND	SUPPLY
11, 45, 59	DVCC	DIGITAL POSITIVE SUPPLY (5 V)	SUPPLY
13	NC		
22	COM1	DAC'S INPUT SELECT	I
36	COM0	DAC'S INPUT SELECT	I
23, 24	A0, A1	CHROMINANCE FILTER CUTOFF SELECT	I
26	X1.3	D2–MAC COMPENSATION SELECT	I
27	O/E F	1/2 CK DELAY PROGRAMMATION (ODD/EVEN FRAME)	I
28..35	B[7..0]	BLUE DIGITAL PROGRAMMABLE BUS	I/O
37..44	G[7..0]	GREEN DIGITAL PROGRAMMABLE BUS	I/O
60..67	R[0..7]	RED DIGITAL PROGRAMMABLE BUS	I/O
58	NC		
48	BAGND	BLUE ANALOG GROUND	SUPPLY
49	BLUE	BLUE ANALOG OUTPUT	O
50	GAGND	GREEN ANALOG GROUND	SUPPLY
51	GREEN	GREEN ANALOG OUTPUT	O
52	AVCC	ANALOG POSITIVE SUPPLY (5V)	SUPPLY
53	RAGND	RED ANALOG GROUND	SUPPLY
54	RED	RED ANALOG OUTPUT	SUPPLY
55	REXT	DAC CURRENT REGULATION	O
46	VREF2	MAIN REFERENCE VOLTAGE (VREF2 – VREF1 = 815 mV)	O
57	VREF1	LOWER REFERENCE VOLTAGE	O
47	TRIM	VREF1 TRIMMING POINT	I

Functional Description

Digital Part

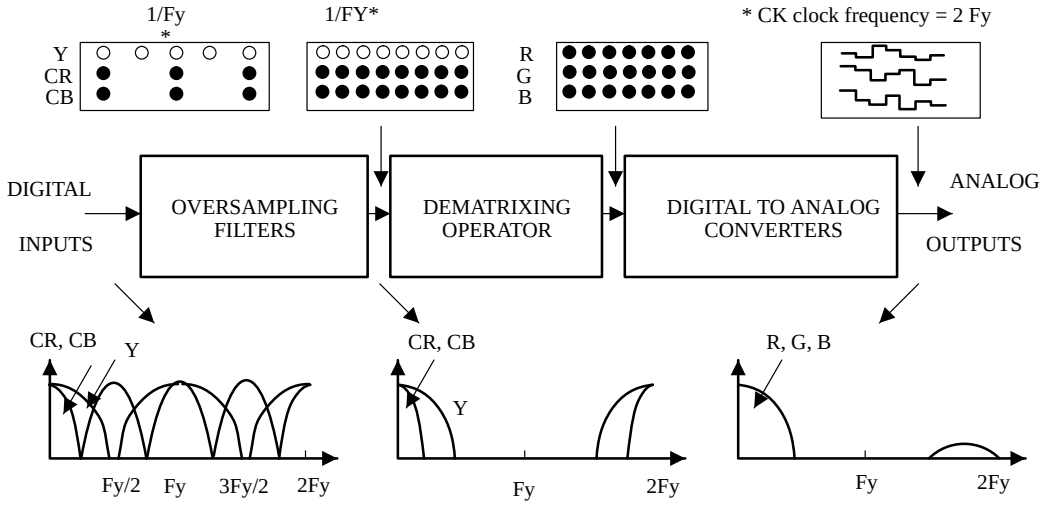
The digital part includes two stages : the first one is a filter increasing the sampling rates of the luminance and the chrominance, and the second one is a video matrix operator which performs the conversion of the over-sampled Y, CR, CB into R, G, B components according to CCIR 601 recommendation. Two external clocks are used : CK (27 MHz) for system clock and SYNC for input signals synchronization.



All internal registers are clocked on the falling edge of CK clock. Internal data paths have been scaled to allow output data in the range [0,255/256] for R, G, B and input data in the range [00, FF] for Y, CR, CB. Saturation circuits are used for out of range data, rounding functions are performed before truncation.

The filter block performs an interpolation by two for luminance signal (Y) and by a factor 4 for each chrominance signal CR and CB.

This operation is equivalent to computing of one intermediate point between each incoming luminance sample and three for the two chrominance samples.



In order to be compatible with CCIR 601 all filters must have a linear phase and a flat response within the frequency band (5.5 MHz for Y and 2 MHz for CR and CB). FIR (non recursive) filters with linear phase have been used and no phase correction is required.

Luminance Filter

The luminance filter is a 19th order transversal linear filter :

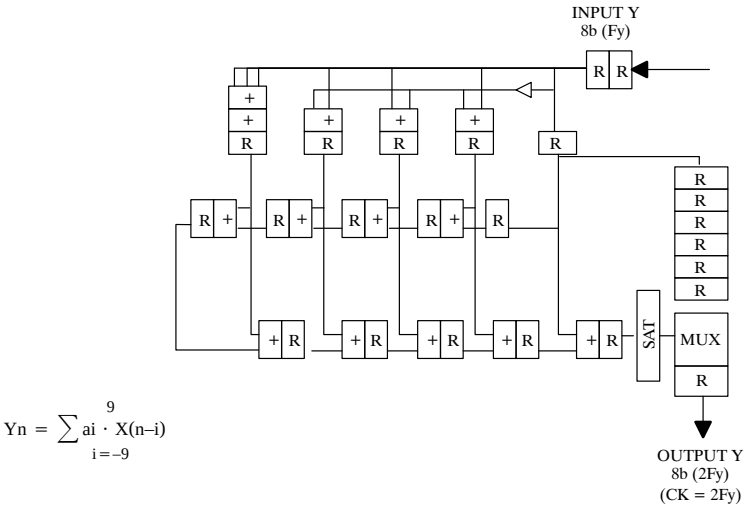
$H(Z) = a0 + a1 (z^1 + z^{-1}) + a3 (z^3 + z^{-3}) + a5 (z^5 + z^{-5)} + a7 (z^7 + z^{-7}) + a9 (z^9 + z^{-9})$

with : a0 = .5
a1 = .328125
a3 = –.117875
a5 = .054687
a7 = –.0234375
a9 = .0078125

The selection of the coefficients takes into account the sin (x)/x attenuation introduced by the DAC's sample-and-hold function.

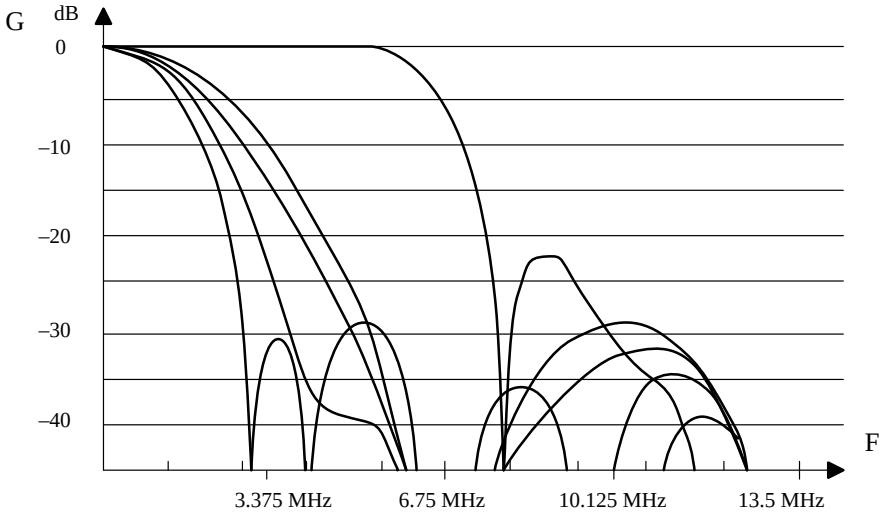
The incoming and outgoing data flows are 8 bit wide with values in the [00, FF] range.

Luminance Filter Block Diagram



$$Yn = \sum_{i=-9}^{9} ai \cdot X(n-i)$$

Luminance and Chrominance Filter Measurements (CK = 27 MHz)



Chrominance Filters

The chrominance filter is made with one 7 th order symetrical filter for multiplexed CR/CB and two separate 2nd order filters for CR and CB.

The 7 th order filter transfer fonction is :

$H(Z) = ho + h1 (Z^1 + Z^{-1}) + h2 (Z^2 + Z^{-2}) + h3 (Z^3 + Z^{-3})$

In a MAC decoder the chrominance filter passband is a compromise between the colour resolution and noise.

For this reason each subfilter is composed of 4 different Bessel filters with a cutoff frequency of 1, 1.3, 1.6 and 2 MHz. The real time noise measurement on a MAC test line can be used to select one of the four colour filters through A0, A1 pins.

A0	A1	CUTOFF
0	0	1 MHz
0	1	1.3 MHz
1	0	1.6 MHz
1	1	2 MHz

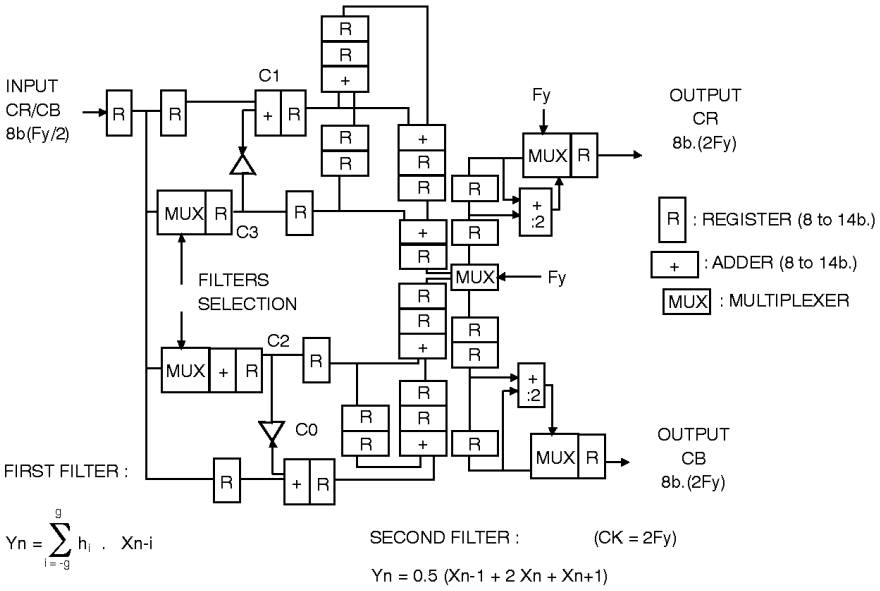
The corresponding coefficients are :

h01 = .011110 h02 = .10010 h03 = .10110 h04 = .11010
h11 = .011000 h12 = .01110 h13 = .01111 h14 = .10010
h21 = .010001 h22 = .00111 h23 = .00101 h24 = .00011
h31 = .001000 h32 = .00010 h33 = .00001 h34 = -.00010

The second order filter transfer function is :

$H(Z) = .5(Z + 2 + Z^{-1})$

Chrominance Filter Block Diagram



Matrix Operator

The matrix operator is in charge of Y, CR, CB → R, G, B conversion according to CCIR 601 recommendation.

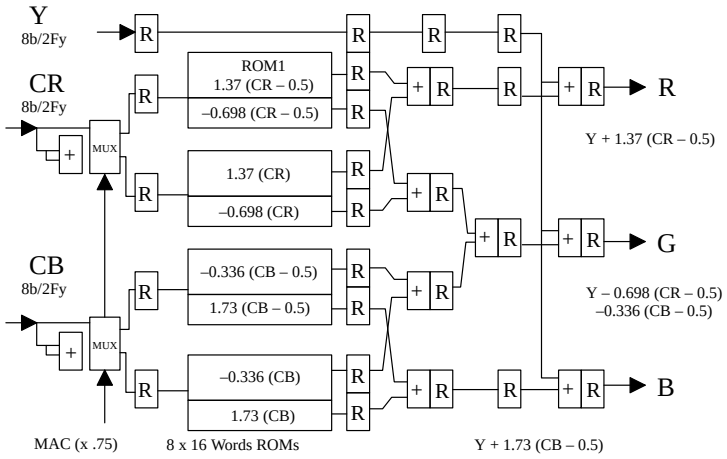
$R = 1.000 \times Y + 1.370 \times (CR–.5) + .000 \times (CB–.5)$

$G = 1.000 \times Y –.698 \times (CR–.5) –.336 \times (CB–.5)$

$B = 1.000 \times Y + .000 \times (CR–.5) + 1.730 \times (CB–.5)$

A ROM architecture has been used to achieve fast multiplications (27 MHz). In order to improve speed this 256-word ROM has been split into 8 × 16-word ROM's.

Dematrixing Operator Architecture and 1.333... Division



The R, G, B signal can be delayed by 1 Clock Period at the output of the matrix operator using the O/E F external command in order to allow frame interleaving in staggered rows.

O/EF	DELAY
0	no delay
1	1 Clock delay (37 nS at 27 MHz)

In order to improve signal/noise ratio and according to the D2-MAC standard the chrominance signals are multiplied by 1.333 before transmission.

A compensation (multiplication by .75 of R, G, B) can be programmed on the reception side through × 1.3 pin.

X 1.3	MULT. FACTOR
0	multiplication by .75
1	no multiplication

Analog Part

Three 8bit D to A converters deliver analog R, G, B signals. Each converter is based on a resistor string used as a voltage divider. The internal reference voltage for the 3 converters is $V_{REF2} - V_{REF1} = 815$ mV. This voltage corresponds to the standard 700 mV range of a video signal from black to white (levels 16 and 235 in CCIR 601). In order to reduce the diaphony between the DAC's, these shared reference voltages are filtered by on chip capacitors. However, additional 1 µF capacitors are required on VREF1, VREF2 and TRIM for better decoupling, and stability.

Each of the three DAC outputs is connected to an operational amplifier used as a unity-gain buffer to drive 75 ohms/20 pF loads.

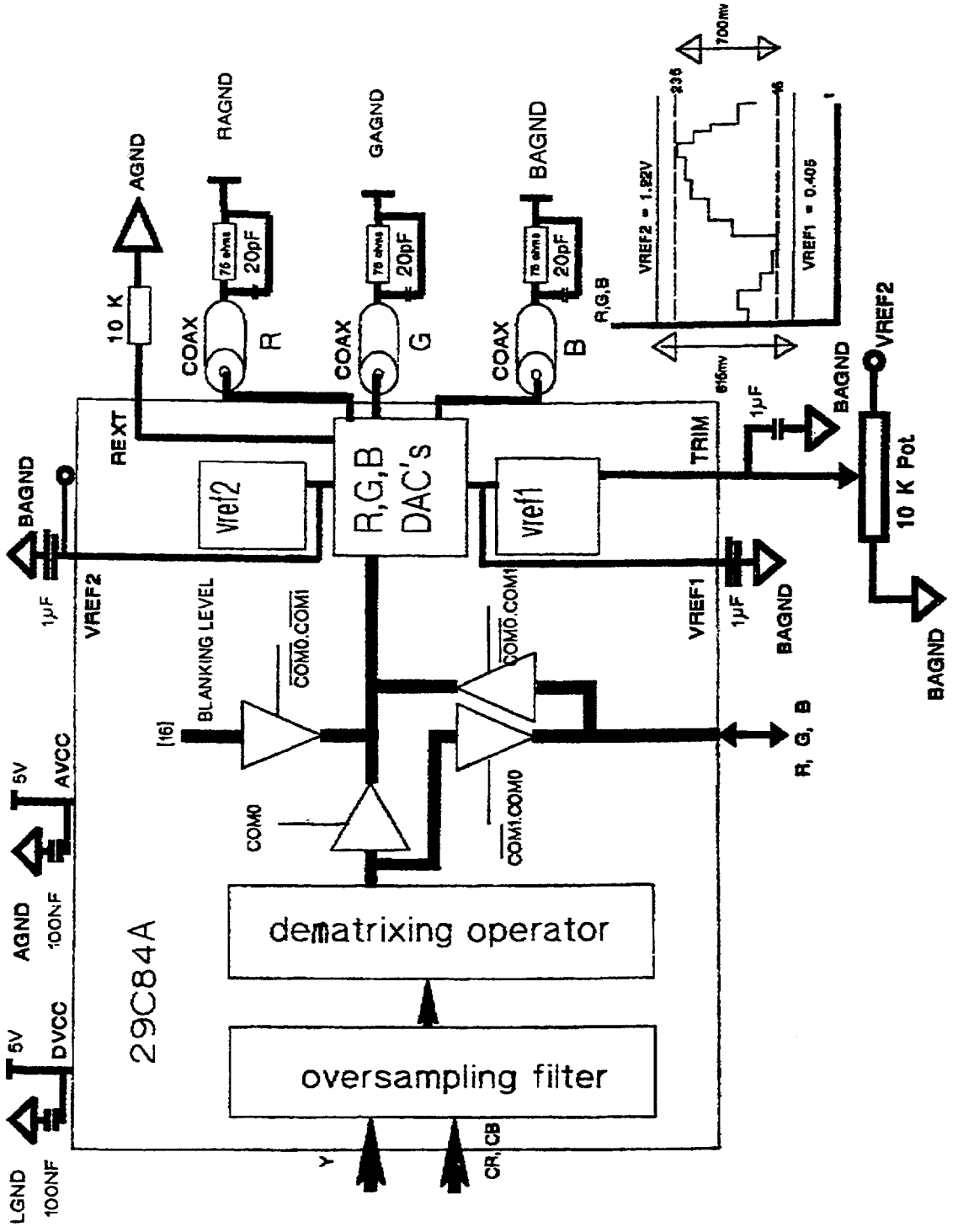
The REXT pin must be tied to a 10 k resistor under normal conditions. Changing the value of REXT modifies output amplifier characteristics (slew rate, passband ...).

3 optional intermediate input/output ports have been implemented between the matrix operator and the DAC's. The converters inputs can be connected to external digital R, G, B sources. This connection is programmed through C0, C1 pins. A typical application in this mode is videotext where TV picture and alphanumeric characters defined by their R, G, B components have to be mixed.

The input/output ports can be programmed as follows :

COM1	COM0	DAC Programmation
1	1	FILTER + DEMATRIXING + DAC mode. Internal filters are connected to DAC inputs.R[0..7], G[0..7], B[0..7] bus are floating.
1	0	TRIPLE/DAC MODE. Filters are not connected to DAC's. R[0..7], G[0..7], B[0..7] are connected to DAC inputs
0	1	FILTER + DEMATRIXING + DAC + MONITORING MODE. Filters are connected to DAC inputs and to R[0..7], G[0..7], B[0..7] bus
0	0	BLANKING MODE DACs inputs are forced to 16 (blanking level) and R[0..7], G[0..7], B[0..7] are floating.

Application Information



Electrical Characteristics

Absolute Maximum Ratings

VCC to GND : . . . . . –0.5 V to + 7 V
input/output voltage : . . . . . –0.3 V to VCC + 0.3 V
storage temperature : . . . . . –65 to 150 °C

Operating Conditions

Voltage range : . . . . . 4.5 to 5.5 V
Temperature range : . . . . . T = 0 to 70°C

DC Electrical Characteristics

VCC = 5 V, T = 25°C
Typical Load for DAC's = 75 Ω, 20 pF

Parameter	Min	Typ	Max	Unit	Conditions
LOW LEVEL INPUT VOLTAGE VIL		.8		V	
HIGH LEVEL INPUT VOLTAGE VIH		3.5		V	
LOW LEVEL OUTPUT VOLTAGE VOL		.4		V	IOL = –4.8MA
HIGH LEVEL OUTPUT VOLTAGE VOH		4		V	IOH = 5MA
LOW LEVEL OUTPUT CURRENT IOL		4.8		MA	VOL = 0.4V
HIGH LEVEL OUTPUT CURRENT IOH		5		MA	VOL = 2.4V
INPUT LEAKAGE CURRENT IIL/IIH		5		UA	VIN = VCC OR 0V
OPERATING CURRENT ICCD		90		MA	LOAD = 75 0HMS OUTPUT CODE = 80 H
OUTPUT OPAMP SLEW RATE	70	100	140	V/US	IO – 90 % OF THE 00H TO FFH
OUTPUT AMP UNITY GBW	25	45	60	MHz	
DAC'S ABSOLUTE LINEARITY			.5	LSB	DIFFERENTIAL AND INTEGRAL
DIAPHONY BETWEEN DACS			–75 –45	DB DB	LOW FREQ 10 KHz HIGH FREQ 1 MHz
GLITCH ENERGY		30		NS.LSB	TRANSITION $80_H \rightarrow 7F_H$
HARMONIC DISTORSION		50		DB	200 KHz
PSRR (All Analog Pins)		50 30		DB DB	LOW FREQ 10 KHZ HIGH FREQ 1 MHZ
VREF1	0.345	0.405	0.465	V	
VREF2	1.16	1.22	1.28	V	
VREF2–VREF1	775	815	855	mV	
TEMP COEFF OF (VREF2–VREF1)			200	ppm/°C	0-70°C

Timings

AC Electrical Characteristics

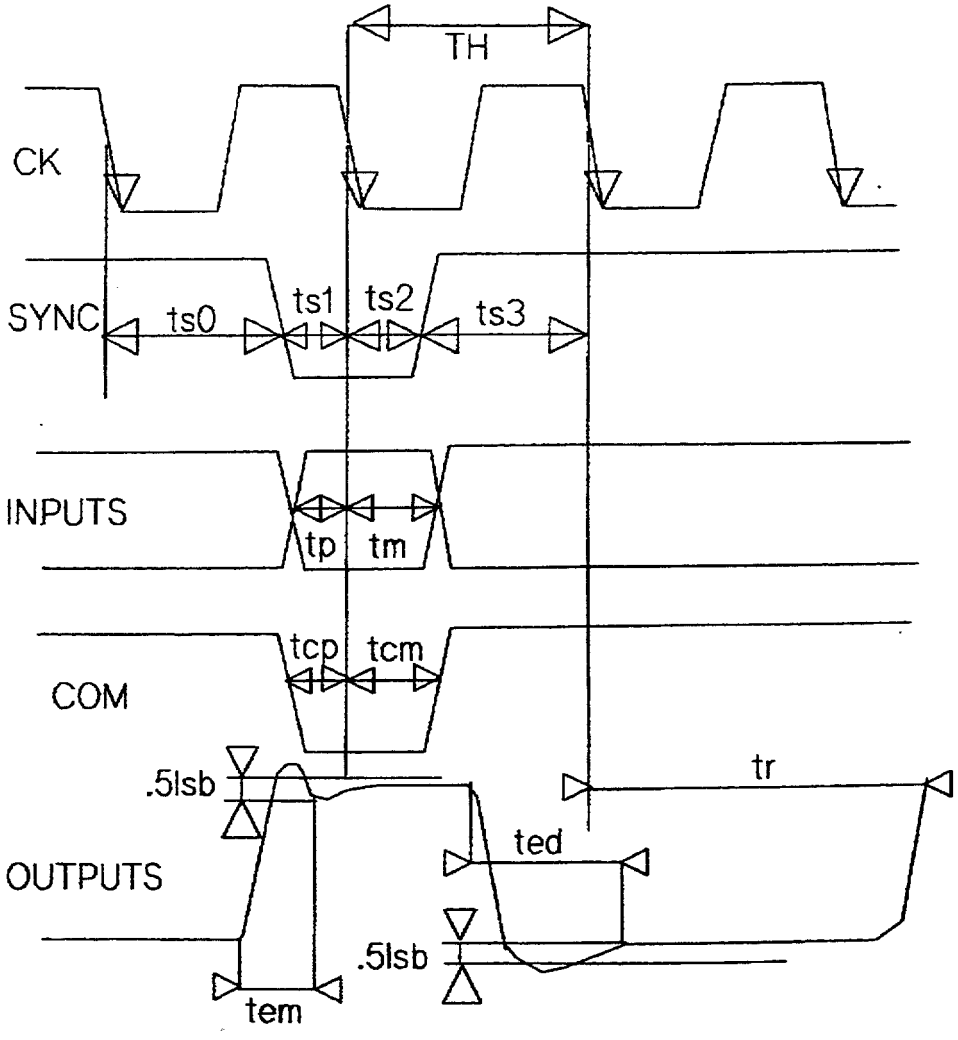
VCC = 5 V ± 10 %, T = 0 to 70°C, CL = 20 pF on R, G, B

Symbol	Parameter	Condition	Min	Typ	Max
tp	input/CK low data setup time		10 ns		
tm	input/CK low data hold time		0 ns		
thmin	minimum CK cycle time		37 ns		
ts0min	CK low to SYNC low		5 ns		
ts1min	SYNC low to CK low		8 ns		
ts2min	CK low to SYNC high		4 ns		
ts3min	SYNC high to CK low		7 ns		
tr max	CK low to R, G, B outputs propagation delay	.5 vref		20 ns	
ted max	DAC settling time full scale to 0	to 1/2 lsb		30 ns	
tem max	DAC settling time 0 to full scale	to 1/2 lsb		20 ns	
tcp	COM [0..1] to CK low setup time		22 ns		
tcm	COM [0..0] from CK low hold time		0 ns		

Application recommendation

The DAC O/P loads should have minimal capacitance load (20 pF typ, 50 pF maximum).

The resistor content can be either 75 Ω or 50 Ω.



Ordering Information

Ø	S	29C84A
TEMPERATURE RANGE Ø COMMERCIAL 0 TO 70 °C I INDUSTRIAL −40 TO 85 °C	PACKAGE : S = PLCC	Part number 29C84A