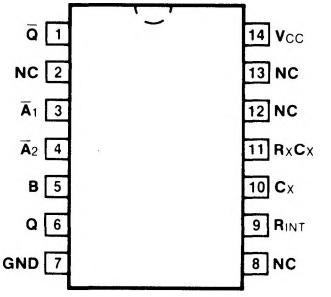
54/74121

MONOSTABLE MULTIVIBRATOR

CONNECTION DIAGRAM
PINOUT A



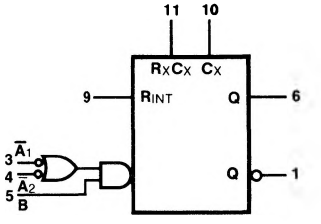
DESCRIPTION — The '121 features positive and negative dc level triggering inputs and complementary outputs. Input pin 5 directly activates a Schmitt circuit which provides temperature compensated level detection, increases immunity to positive-going noise and assures jitter-free response to slowly rising triggers.

When triggering occurs, internal feedback latches the circuit, prevents re-triggering while the output pulse is in progress and increases immunity to negative-going noise. Noise immunity is typically 1.2 V at the inputs and 1.5 V on V_{CC}.

Output pulse width stability is primarily a function of the external R_x and C_x chosen for the application. A 2 kΩ internal resistor is provided for optional use where output pulse width stability requirements are less stringent. Maximum duty cycle capability ranges from 67% with a 2 kΩ resistor to 90% with a 40 kΩ resistor. Duty cycles beyond this range tend to reduce the output pulse width. Otherwise, output pulse width follows the relationship:

$$t_w = 0.69\ R_xC_x$$

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2,8,12,13

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74121PC		9A
Ceramic DIP (D)	A	74121DC	54121DM	6A
Flatpak (F)	A	74121FC	54121FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L.definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\bar{A}_1$, $\bar{A}_2$	Trigger Inputs (Active Falling Edge)	1.0/1.0
B	Schmitt Trigger Input (Active Rising Edge)	2.0/2.0
Q, $\bar{Q}$	Outputs	20/10

TRIGGERING TRUTH TABLE

INPUTS $\bar{A}_1$	INPUTS $\bar{A}_2$	INPUTS B	RESPONSE
H	H	⊓	No Trigger
L	X	⊓	Trigger
X	L	⊓	Trigger
⊔	L	X	No Trigger
⊔	X	L	No Trigger
⊔	H	H	Trigger
L	⊔	X	No Trigger
X	⊔	L	No Trigger
H	⊔	H	Trigger

NOTE:
Triggering occurs only when the $\bar{Q}$ output is HIGH (not in timing cycle) and one of the above triggering situations is satisfied.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
V_{T+}	Positive-going Threshold Voltage at $\bar{A}_n$ or B Inputs			2.0	V	V_{CC} = Min
V_{T-}	Negative-going Threshold Voltage at $\bar{A}_n$ or B Inputs		0.8		V	V_{CC} = Min
I_{OS}	Output Short Circuit Current	XM	-20	-55	mA	V_{CC} = Max
		XC	-18	-55		
I_{CC}	Power Supply Current	Quiescent State		25	mA	V_{CC} = Max
		Fired State		40		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF Min	54/74 C_L = 15 pF Max	UNITS	CONDITIONS	
t_{PLH}	Propagation Delay B to Q	15	55	ns	C_X = 80 pF Fig. 3-1, Fig. a	
t_{PLH}	Propagation Delay $\bar{A}_n$ to Q	25	70	ns		
t_{PHL}	Propagation Delay B to $\bar{Q}$	20	65	ns		
t_{PHL}	Propagation Delay $\bar{A}_n$ to $\bar{Q}$	30	80	ns		
t_W	Pulse Width Using Internal Timing Resistor	70	150	ns	C_X = 80 pF	R_X = Open Fig. 3-1
t_W	Pulse Width with Zero Timing Capacitance	20	50	ns	C_X = 0 pF	Fig. a Pin 9 = V_{CC}
t_W	Pulse Width Using External Timing Resistor	600	800	ns	C_X = 100 pF	R_X = 10 kΩ Pin 9 = Open
		6.0	8.0	ms	C_X = 1.0 μF	Fig. 3-1, a
t_{HOLD}	Minimum Duration of Trigger Pulse		50	ns	C_X = 80 pF, R_X = Open Pin 9 = V_{CC}, Fig. a	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYBMOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
V_{r-f}	Input Pulse Rise/Fall Slew Rate	@ A_n		1.0	V/μs	
		@ B		1.0	V/s	
Rx	External Timing Resistor	XC	1.4	40	kΩ	
		XM	1.4	30		
Cx	External Timing Capacitor		0	1000	μF	
t_w	Output Pulse Width			40	sec	Fig. a
	Duty Cycle	XM,XC		67	%	Rx = 2 kΩ
		XM		90		Rx = 30 kΩ
		XC		90		Rx = 40 kΩ

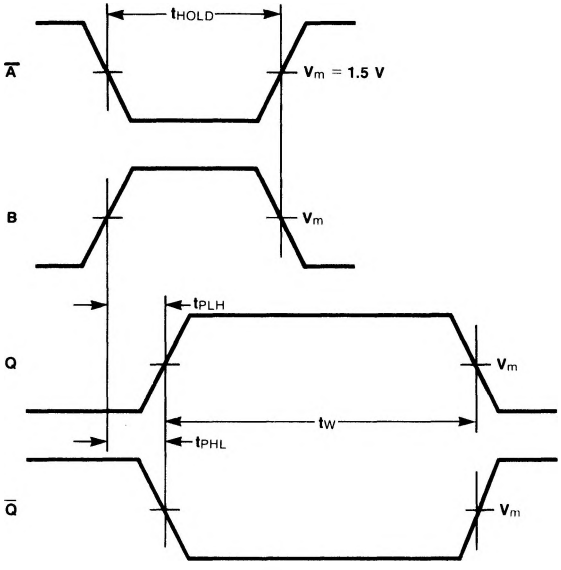


Fig. a

TYPICAL CHARACTERISTICS

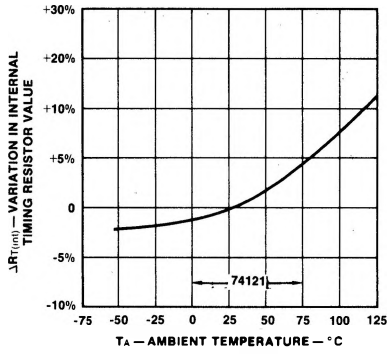


Fig. b Variation in Internal Timing Resistor Value Versus Ambient Temperaure

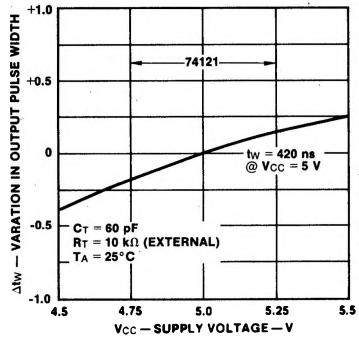


Fig. c Variation in Output Pulse Width Versus Supply Voltage

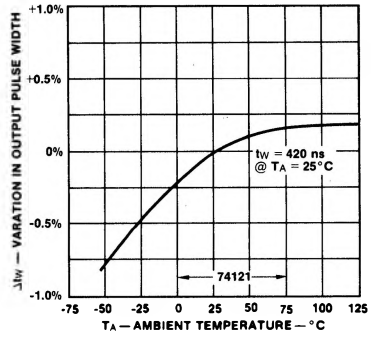


Fig. d Variation in Output Pulse Width Versus Ambient Temperature

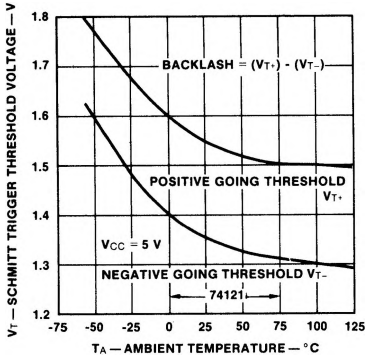


Fig. e Schmitt Trigger Threshold Voltage Versus Ambient Temperature

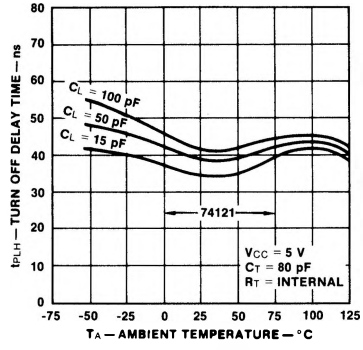


Fig. f Propagation Delay Time B Input to Q Output Versus Ambient Temperature

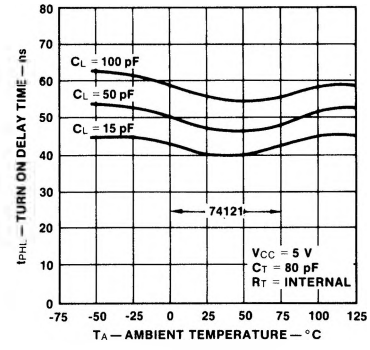


Fig. g Propagation Delay Time B Input to $\overline{Q}$ Output Versus Ambient Temperature

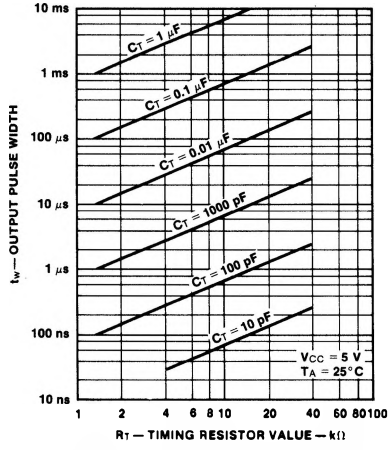


Fig. h Output Pulse Width Versus Timing Resistor Value

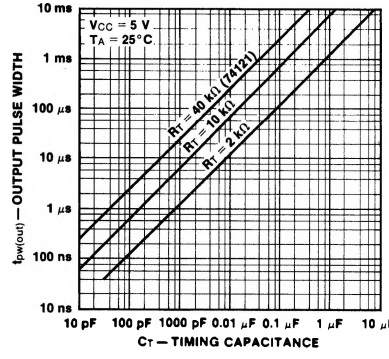


Fig. i Output Pulse Width Versus External Capacitance