54ABT16245 16-Bit Transceiver with TRI-STATE® Outputs

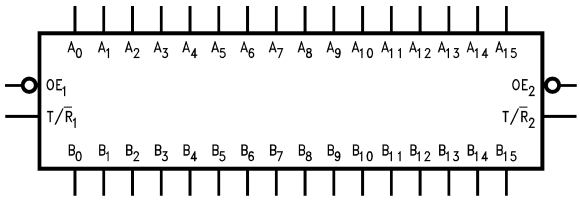
Check for Samples: 54ABT16245

FEATURES

- **Bidirectional non-inverting buffers**
- **Separate control logic for each byte**
- **16-bit version of the 'ABT245**
- **A and B output sink capability of 48 mA, source capability of 24 mA**
- **Guaranteed latchup protection**
- **High impedance glitch free bus loading during entire power up and power down cycle**
- **Non-destructive hot insertion capability**
- **Standard Microcircuit Drawing (SMD) 5962-9317501**

DESCRIPTION

The 'ABT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The T/$\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.



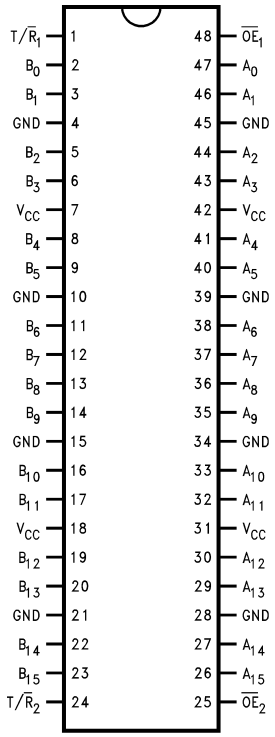
Pin Functions

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
T/$\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/Outputs
B_0–B_{15}	Side B Inputs/Outputs

Connection Diagram

Figure 1. Pin Assignment for Cerpack



Functional Description

The 'ABT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

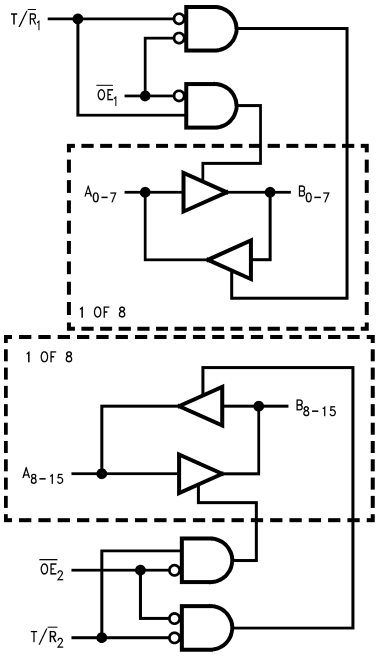
Truth Table(1)

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

(1) H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

Figure 2. Logic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (2)	−0.5V to +7.0V
Input Current (2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

(1) Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
(2) Either voltage limit or current limit is sufficient to protect inputs.

Recommended OperatingConditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V

Recommended OperatingConditions (continued)

Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT16245			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA ($\overline{OE}_n$, T/$\overline{R}_n$)
V_{OH}	Output HIGH Voltage	54ABT	2.5			V	Min	I_{OH} = −3 mA (A_n, B_n)
		54ABT	2.0			V	Min	I_{OH} = −24 mA (A_n, B_n)
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA (A_n, B_n)
I_{IH}	Input HIGH Current				5	µA	Max	V_{IN} = 2.7V ($\overline{OE}_n$, T/$\overline{R}_n$) (1)
					5			V_{IN} = V_{CC} ($\overline{OE}_n$, T/$\overline{R}_n$)
I_{BVI}	Input HIGH Current Breakdown Test				7	µA	Max	V_{IN} = 7.0V ($\overline{OE}_n$, T/$\overline{R}_n$)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				100	µA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current				−5	µA	Max	V_{IN} = 0.5V ($\overline{OE}_n$, T/$\overline{R}_n$) (1)
					−5			V_{IN} = 0.0V ($\overline{OE}_n$, T/$\overline{R}_n$)
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA ($\overline{OE}_n$, T/$\overline{R}_n$)All Other Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current				50	µA	0 − 5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current				−50	µA	0 − 5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V (A_n, B_n)
I_{CEX}	Output High Leakage Current				50	µA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test				100	µA	0.0	V_{OUT} = 5.50V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current				100	µA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				100	µA	Max	$\overline{OE}_n$ = V_{CC}, T/$\overline{R}_n$ = GND or V_{CC} All others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V $\overline{OE}_n$, T/ R_n V_I = V_{CC} − 2.1V Data Input V_I = V_{CC} − 2.1V All others at V_{CC} or GND
		Outputs TRI-STATE			2.5	mA		
		Outputs TRI-STATE			50	µA		
I_{CCD}	Dynamic I_{CC}	No Load			0.1	mA/MHz	Max	Outputs Open $\overline{OE}_n$ = GND, T/$\overline{R}_n$ = GND or V_{CC} One Bit Toggling, 50% Duty Cycle

(1) Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units	Fig. No.
		T_A =			
		−55°C to +125°C			
		V_{CC} = 4.5V–5.5V			
		C_L = 50 pF			
		Min	Max		
t_{PLH}	Propagation Delay Data to Outputs	0.5	4.5	ns	Figure 5
t_{PHL}		0.5	5.2		
t_{PZH}	Output Enable Time	0.8	6.4	ns	Figure 4
t_{PZL}		0.9	6.9		
t_{PHZ}	Output Disable Time	1.3	6.9	ns	Figure 4
t_{PLZ}		1.0	6.9		

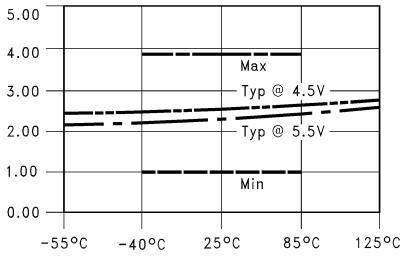
Capacitance

Symbol	Parameter	Typ	Units	Conditions, T_A = 25°C
C_{IN}	Input Capacitance	5	pF	V_{CC} = 0.0V ($\overline{OE}_n$, T/$\overline{R}_n$)
$C_{I/O}$ (1)	Output Capacitance	11	pF	V_{CC} = 5.0V (A_n, B_n)

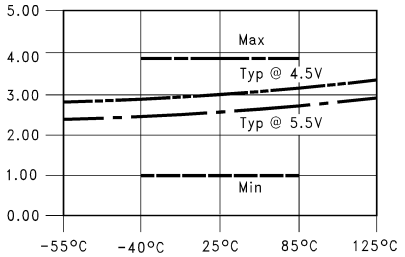
(1) $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Typical Characteristics

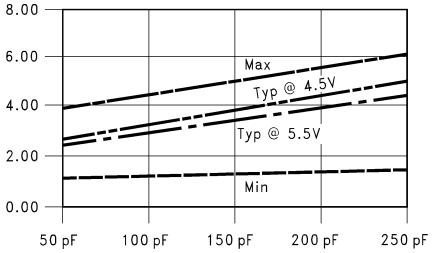
t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



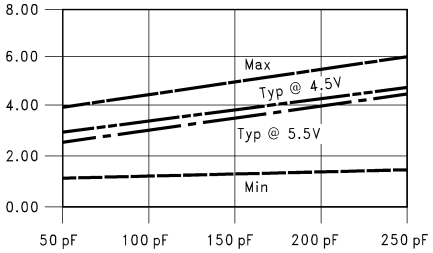
t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



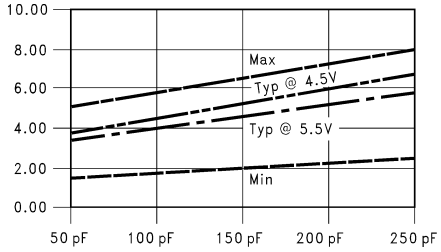
t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C



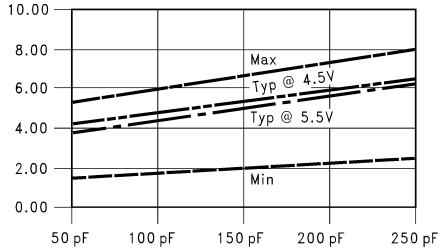
t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C



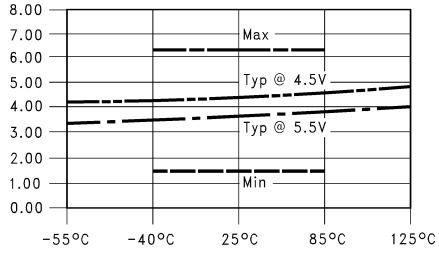
t_{PLH} vs Load Capacitance
16 Outputs Switching, T_A = 25°C



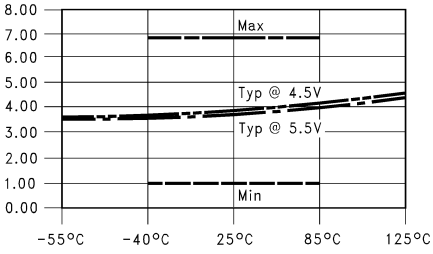
t_{PHL} vs Load Capacitance
16 Outputs Switching, T_A = 25°C



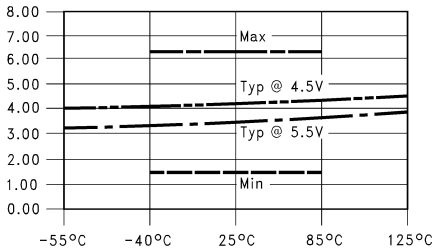
t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



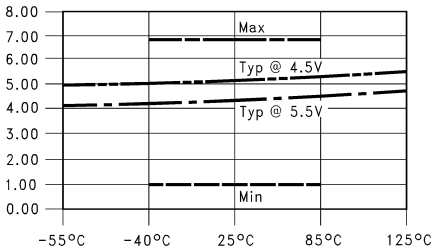
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



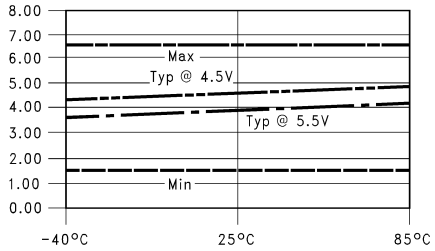
t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



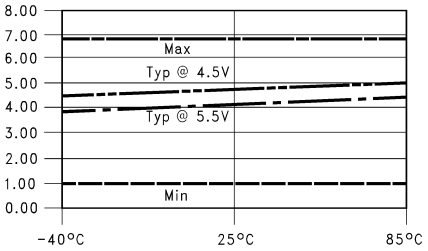
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



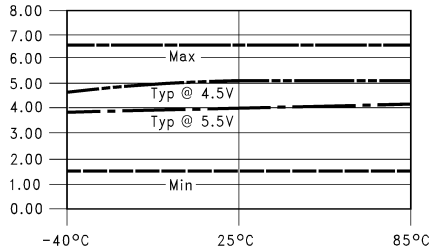
t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



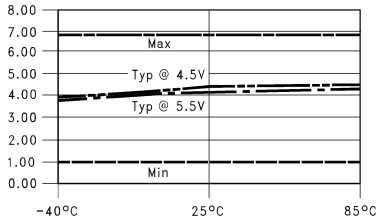
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



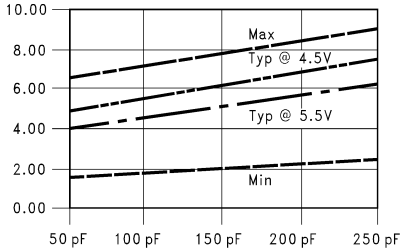
t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



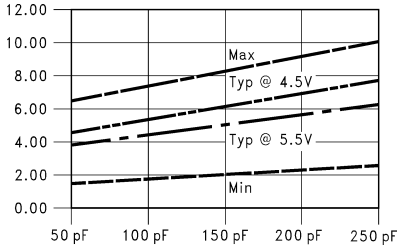
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 16 Outputs Switching



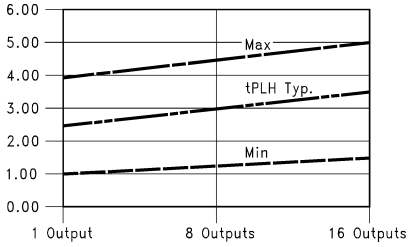
t_{PZL} vs Load Capacitance
16 Outputs Switching T_A = 25°C



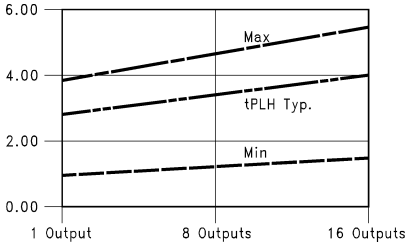
t_{PZH} vs Load Capacitance
16 Outputs Switching T_A = 25°C



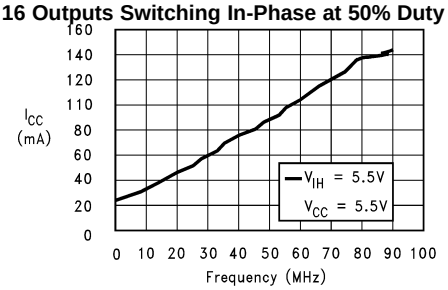
t_{PLH} vs Number Output Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



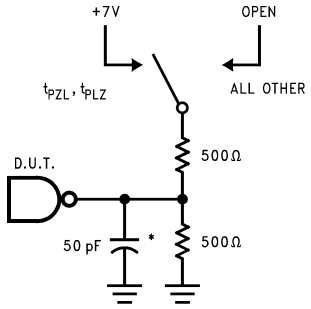
t_{PHL} vs Number Output Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



I_{CC} vs Frequency
Average, T_A = 25°C, V_{CC} = 5.5V
All Outputs Unloaded/Unterminated;
16 Outputs Switching In-Phase at 50% Duty Cycle



AC Loading



*Includes jig and probe capacitance

Standard AC Test Load

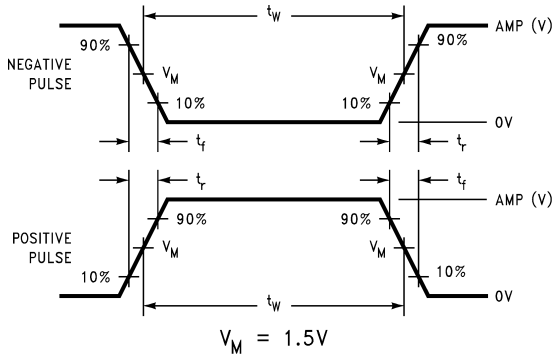


Figure 3. Input Pulse Requirements

Table 1. Test Input Signal Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

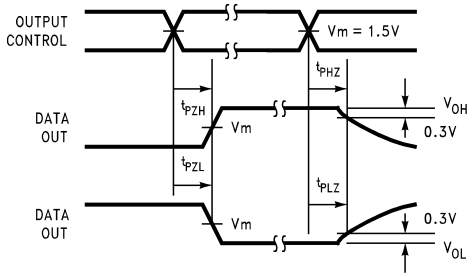


Figure 4. TRI-STATE Output HIGH and LOW Enable and Disable Times

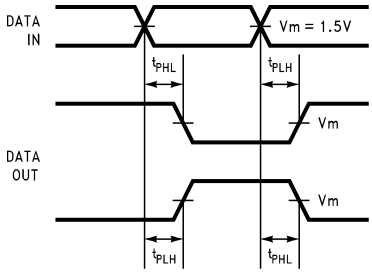


Figure 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

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