54ABT16374

54ABT16374 16-Bit D Flip-Flop with TRI-STATE Outputs

Literature Number: SNOS051A

National Semiconductor

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54ABT16374
16-Bit D Flip-Flop with TRI-STATE® Outputs

General Description

The ABT16374 contains sixteen non-inverting D flip-flops with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable ($\overline{OE}$) are common to each byte and can be shorted together for full 16-bit operation.

Features

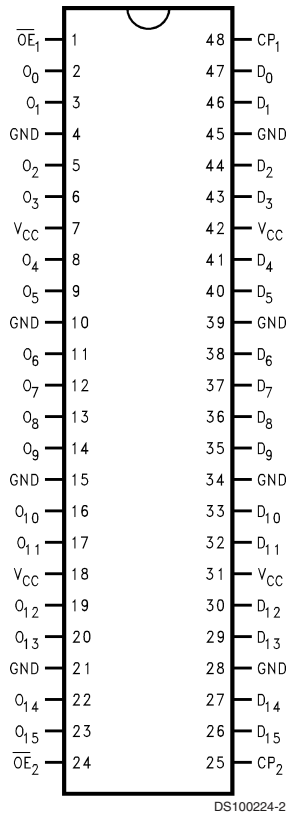
- Separate control logic for each byte
- 16-bit version of the ABT374
- Edge-triggered D-type inputs
- Buffered Positive edge-triggered clock
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Guaranteed latch-up protection
- Standard Microcircuit Drawing (SMD) 5962-9320101

Ordering Code:

Commercial	Package Number	Package Description
54ABT16374W-QML	WA48A	48-Lead Cerpack

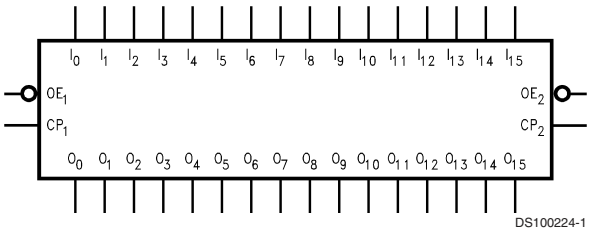
Connection Diagram

Pin Assignment for Cerpack



DS100224-2

Logic Symbol



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Pin Description

Pin Names	Description
$\overline{OE}_n$	TRI-STATE Output Enable Input (Active Low)
CP_n	Clock Pulse Input (Active Rising Edge)
D_0–D_{15}	Data Inputs
O_0–O_{15}	TRI-STATE Outputs

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Functional Description

The ABT16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable ($\overline{OE}_n$) LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}_n$ is HIGH, the outputs go to the high impedance state. Operation of the OE_n input does not affect the state of the flip-flops.

Truth Tables

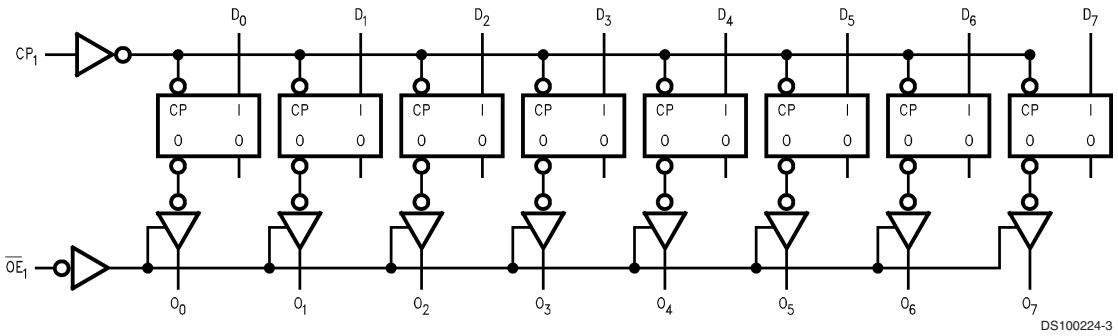
Inputs			Outputs
CP_1	$\overline{OE}_1$	D_0–D_7	O_0–O_7
N	L	H	H
N	L	L	L
L	L	X	(Previous)
X	H	X	Z

Inputs			Outputs
CP_2	$\overline{OE}_2$	D_8–D_{15}	O_8–O_{15}
N	L	H	H
N	L	L	L
L	L	X	(Previous)
X	H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagrams

Byte 1 (0:7)



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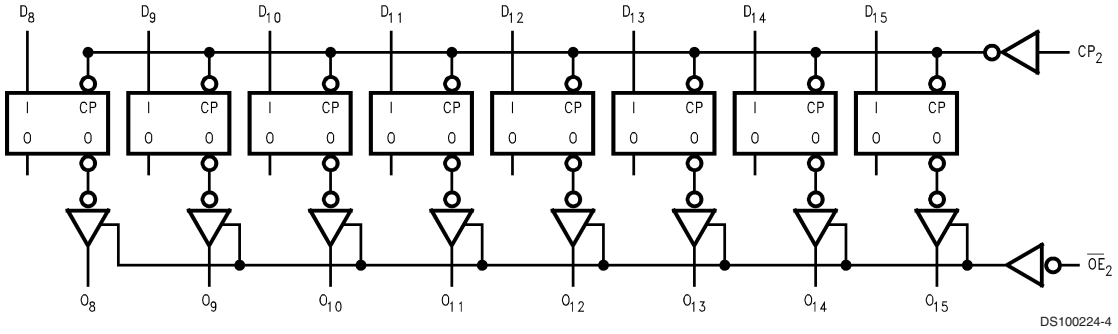
Byte 2 (8:15)



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Absolute Maximum Ratings (Note 1)

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current:	
$\overline{OE}$ Pin	−350 mA
(Across Comm Operating Range)	
Other Pins	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		ABT16374 Min	ABT16374 Typ	ABT16374 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −24 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V (Note 4)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V (Note 4)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA
								All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0–5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0–5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others V_{CC} or GND
I_{CCH}	Power Supply Current				2.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				62	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				2.0	mA	Max	$\overline{OE}$ = V_{CC}; All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA		V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA	Max	Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Data Input V_I = V_{CC} − 2.1V
								All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC}	No Load				mA/	Max	Outputs Open
	(Note 4)				0.30	MHz		$\overline{OE}$ = GND, (Note 3)
								One Bit Toggling, 50% Duty Cycle

Note 3: For 8-bit toggling, I_{CCD} < 0.8 mA/MHz.

Note 4: Guaranteed, but not tested.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		1.1	V	5.0	T_A = 25˚C (Note 5)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}		-0.45	V	5.0	T_A = 25˚C(Note 5)

Note 5: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW.

AC Electrical Characteristics

Symbol	Parameter	54ABT T_A = –55˚C to +125˚C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units
		Min	Max	
f_{max}	Max Clock Frequency	150		MHz
t_{PLH}	Propagation Delay	1.5	6.9	ns
t_{PHL}	CP to O_n	1.5	6.9	
t_{PZH}	Output Enable Time	0.8	6.5	ns
t_{PZL}		1.2	6.5	
t_{PHZ}	Output Disable Time	1.5	9.6	ns
t_{PLZ}		1.5	7.2	

AC Operating Requirements

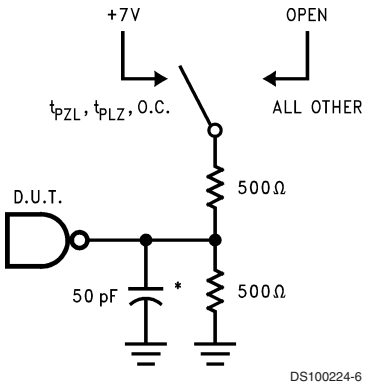
Symbol	Parameter	54ABT T_A = –55˚C to +125˚C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units
		Min	Max	
t_s(H)	Setup Time, HIGH	1.3		ns
t_s(L)	or LOW D_n to CP	1.3		
t_h(H)	Hold Time, HIGH	1.5		ns
t_h(L)	or LOW D_n to CP	1.5		
t_w(H)	Pulse Width, CP	3.3		ns
t_w(L)	HIGH or LOW	3.3		

Capacitance

Symbol	Parameter	Typ	Units	Conditions (T_A = 25˚C)
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 0V
C_{OUT} (Note 6)	Output Capacitance	11.0	pF	V_{CC} = 5.0V

Note 6: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

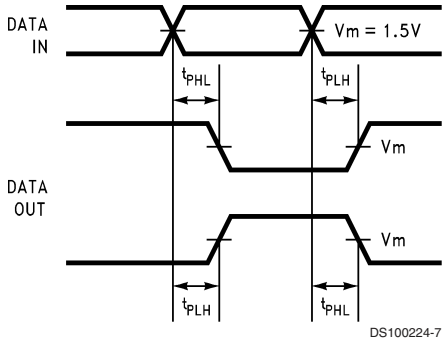


FIGURE 2. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

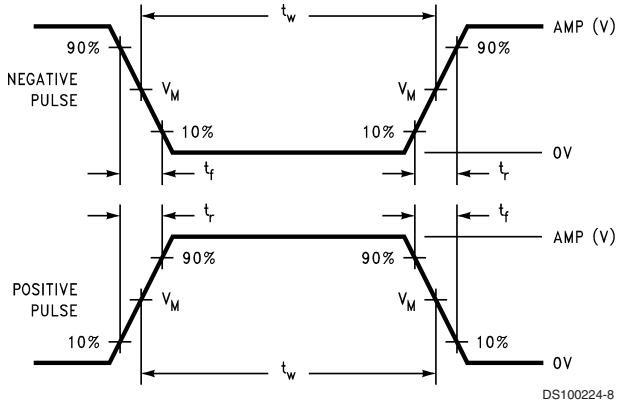


FIGURE 3. Test Input Pulse Requirements

Amplitude	Rep Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 4. Test Input Signal Requirements

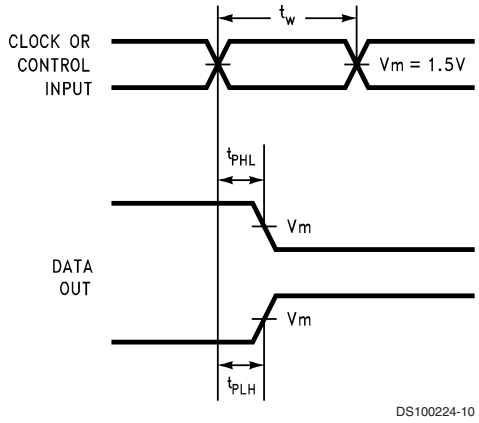


FIGURE 5. Propagation Delay, Pulse Width Waveforms

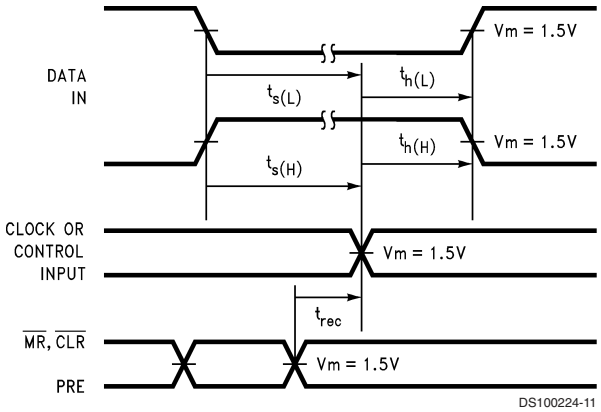


FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

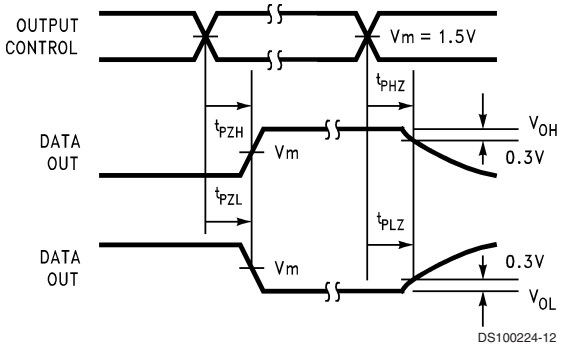
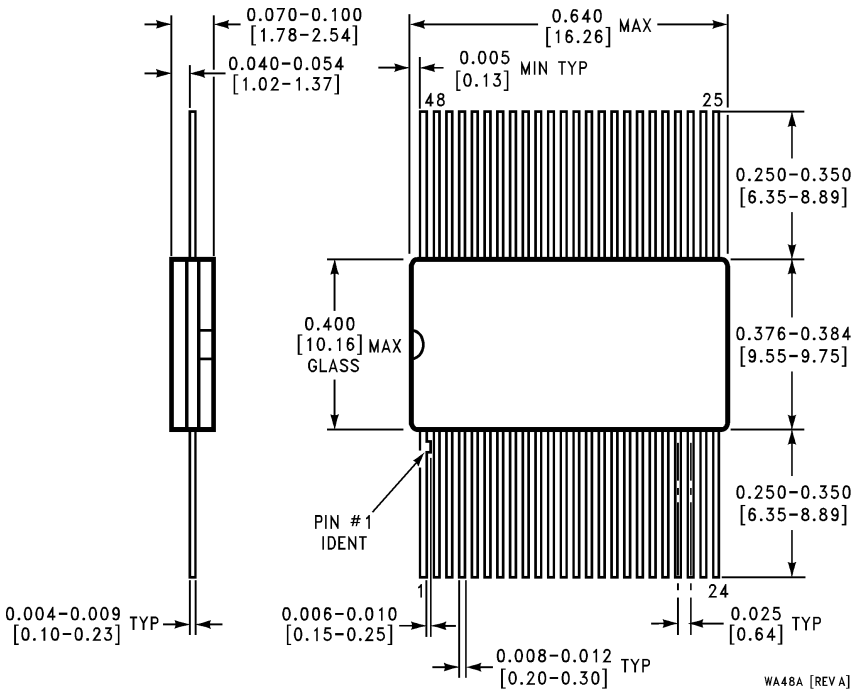


FIGURE 7. TRI-STATE Output HIGH and LOW Enable and Disable Times

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Cerpack
NS Package Number WA48A

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