54ABT541 Octal Buffer/Line Driver with TRI-STATE® Outputs

Check for Samples: 54ABT541

FEATURES

- **Non-inverting buffers**
- **Output sink capability of 48 mA, source capability of 24 mA**
- **Guaranteed latchup protection**
- **High impedance glitch free bus loading during entire power up and power down cycle**
- **Nondestructive hot insertion capability**
- **Flow-through pinout for ease of PC board layout**
- **Disable time less than enable time to avoid bus contention**
- **Standard Microcircuit Drawing (SMD) 5962-9471801**

DESCRIPTION

The 'ABT541 is an octal buffer and line driver with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The 'ABT541 is similar to the 'ABT244 with broadside pinout.

Military	Package Number	Package Description
54ABT541J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT541W-QML	W20A	20-Lead Cerpack
54ABT541E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagram

Figure 1. Pin Assignment DIP and Cerpack

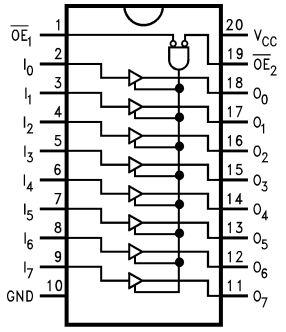
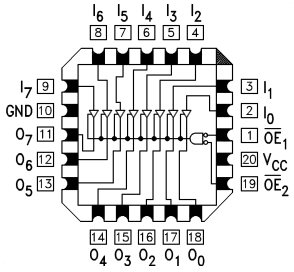


Figure 2. Pin Assignment LCC



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Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active Low)
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Table
(1)

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	ABT541
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

(1) H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (2)	−0.5V to +7.0V
Input Current (2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

(1) Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
(2) Either voltage limit or current limit is sufficient to protect inputs.

Recommended OperatingConditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT541			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −24 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
I_{IH}	Input HIGH Current				5	µA	Max	V_{IN} = 2.7V (1)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current				7	µA	Max	V_{IN} = 7.0V
	Breakdown Test							
I_{IL}	Input LOW Current				−5	µA	Max	V_{IN} = 0.5V (1)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA
								All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	µA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}_n$ = 2.0V
I_{OZL}	Output Leakage Current				−50	µA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}_n$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	µA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				50	µA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	µA	Max	$\overline{OE}_n$ = V_{CC};
								All Others at V_{CC} or Ground
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA		V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA	Max	Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			50	µA		Data Input V_I = V_{CC} − 2.1V;
								All Others at V_{CC} or Ground
I_{CCD}	Dynamic I_{CC}	No Load				mA/	Max	Outputs Open, $\overline{OE}_n$ = GND,
	(1)				0.1	MHz		One Bit Toggling (2),
								50% Duty Cycle

(1) Guaranteed, but not tested.
(2) For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V_{CC}	Conditions
						C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		1.0	V	5.0	T_A = 25°C (1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}		-1.45	V	5.0	T_A = 25°C (1)

(1) Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

AC Electrical Characteristics

		54ABT			
		T_A = −55°C to +125°C			Fig.
Symbol	Parameter	V_{CC} = 4.5V–5.5V		Units	No.
		C_L = 50 pF			
		Min	Max		
t_{PLH}	Propagation Delay	1.0	5.0	ns	Figure 23
t_{PHL}	Data to Outputs	1.0	5.3		
t_{PZH}	Output Enable Time	1.1	7.2	ns	Figure 24
t_{PZL}		1.5	7.9		
t_{PHZ}	Output Disable Time	1.5	7.5	ns	Figure 24
t_{PLZ}		1.5	7.9		

Capacitance

Symbol	Parameter	Typ	Units	Conditions
				T_A = 25°C
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 0.0V
C_{OUT} (1)	Output Capacitance	9.0	pF	V_{CC} = 5.0V

(1) C_{OUT} is measured at frequency of f = 1 MHz, per MIL-STD-883B, Method 3012.

Figure 3. t_{PLH} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching

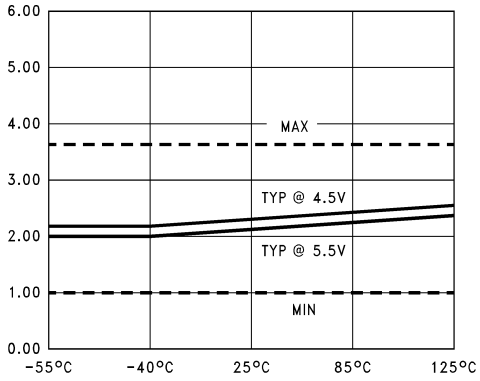


Figure 4. t_{PHL} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching

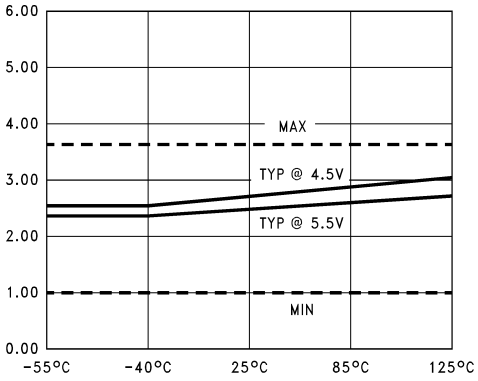


Figure 5. t_{PLH} vs Load Capacitance 1 Output Switching, T_A = 25°C

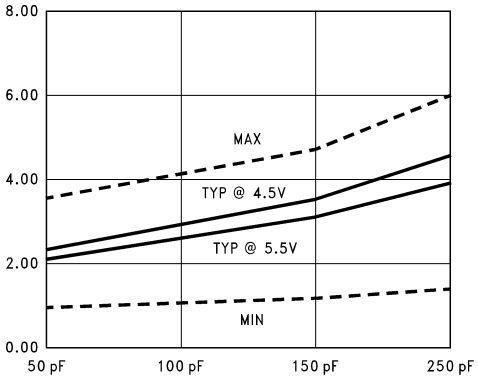


Figure 6. t_{PHL} vs Load Capacitance 1 Output Switching, T_A = 25°C

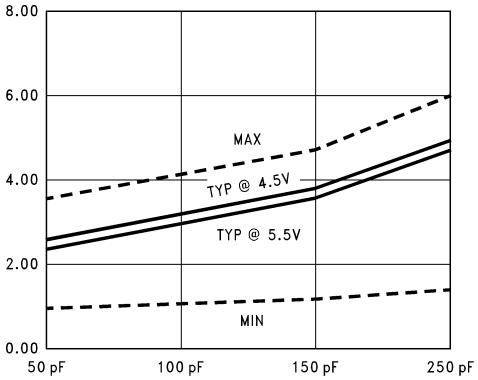


Figure 7. t_{PLH} vs Load Capacitance 8 Outputs Switching, T_A = 25°C

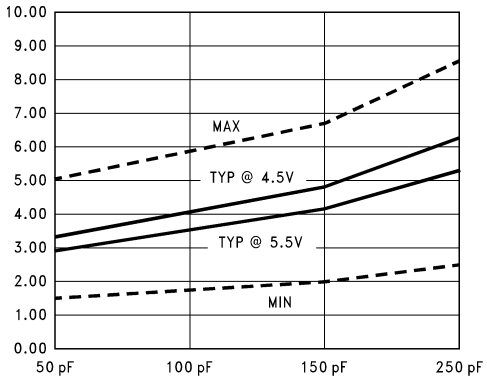
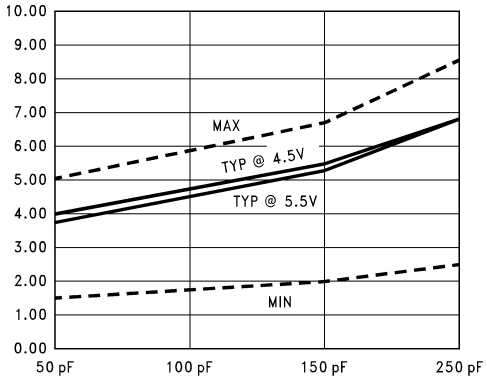


Figure 8. t_{PHL} vs Load Capacitance 8 Outputs Switching, T_A = 25°C



Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

Figure 9. t_{PZL} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching

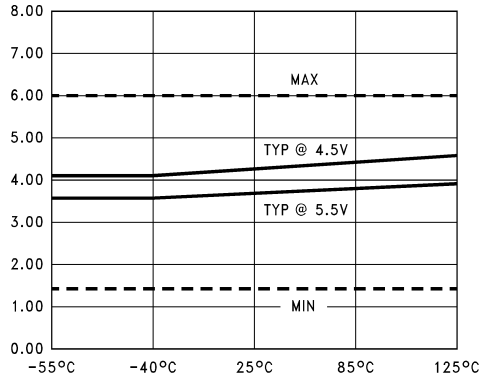


Figure 10. t_{PLZ} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching

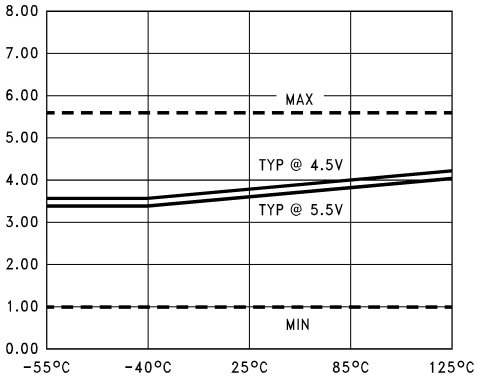


Figure 11. t_{PZL} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching

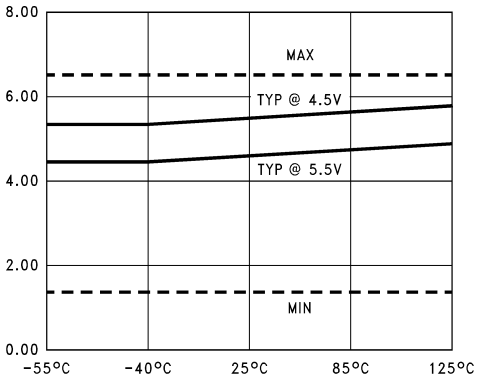


Figure 12. t_{PLZ} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching

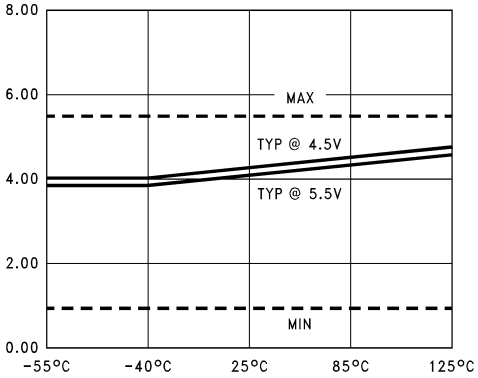


Figure 13. t_{PZH} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching

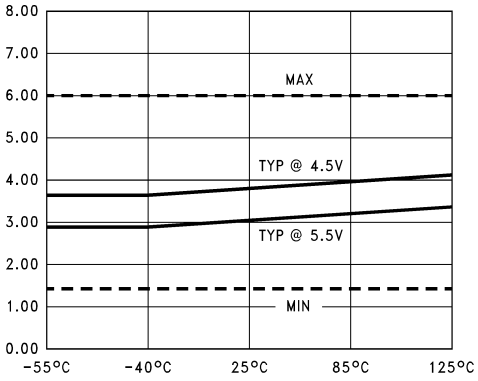
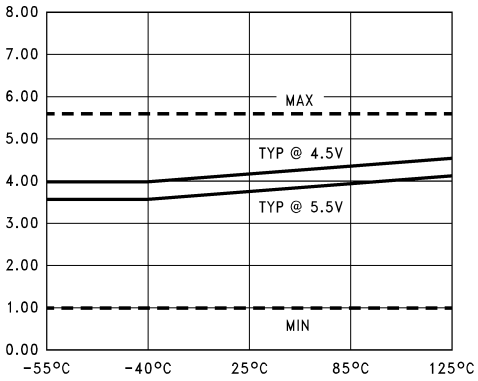


Figure 14. t_{PHZ} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching



Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

Figure 15. t_{PZH} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching

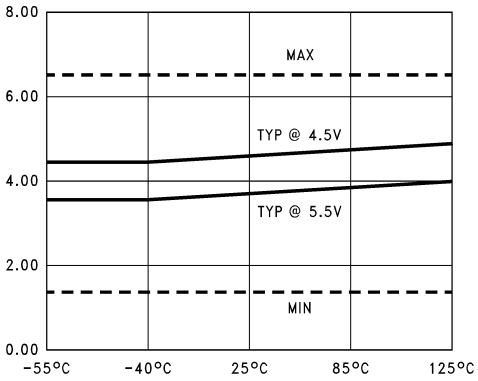


Figure 16. t_{PHZ} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching

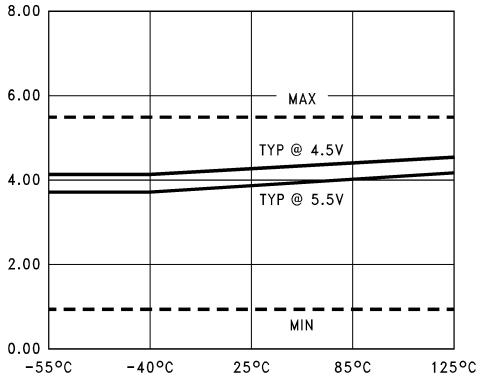


Figure 17. t_{PZH} vs Load Capacitance 8 Outputs Switching, T_A = 25°C

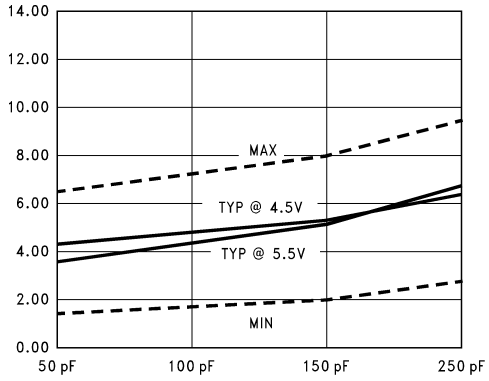


Figure 18. t_{PZL} vs Load Capacitance 8 Outputs Switching, T_A = 25°C

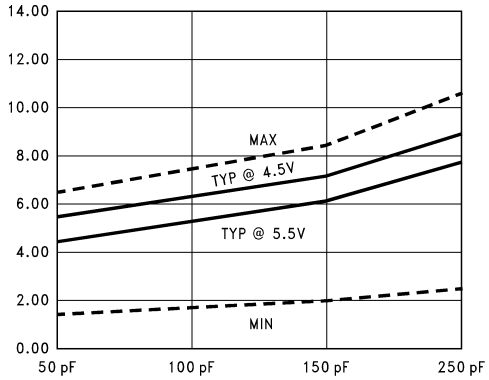


Figure 19. t_{PLH} and t_{PHL} vs Number Outputs Switching V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF

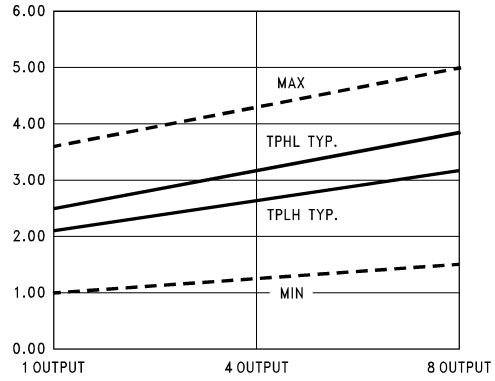
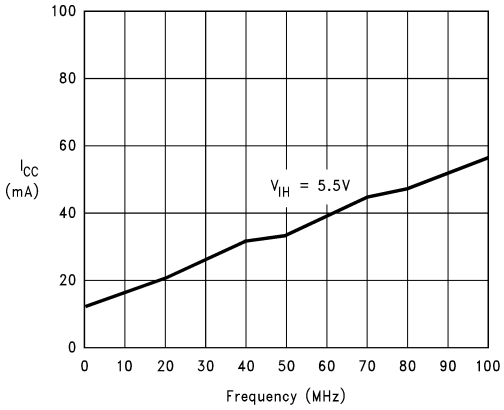


Figure 20. I_{CC} vs Frequency, Average, T_A = 25°C, All Outputs Unloaded/Unterminated



Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

AC Loading

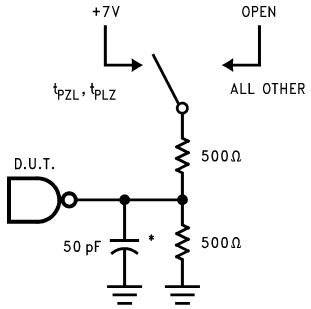


Figure 21. Standard AC Test Load

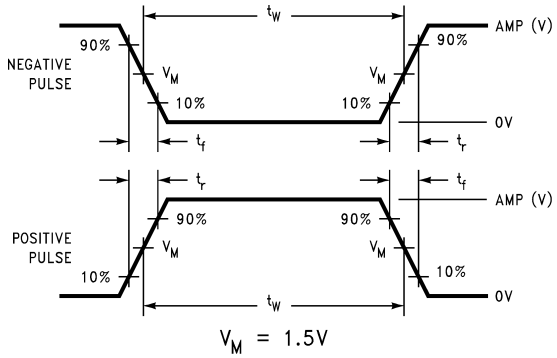


Figure 22. Test Input Signal Levels

Test Input Signal Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

AC Waveforms

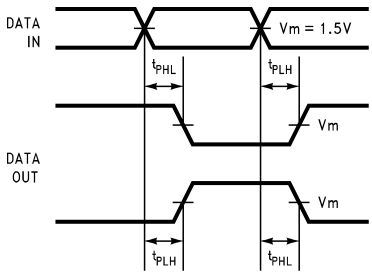


Figure 23. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

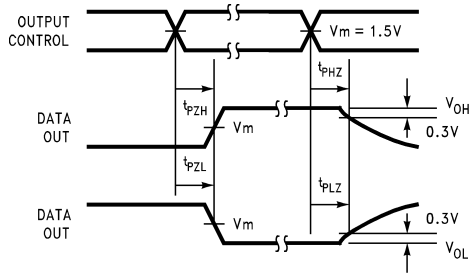


Figure 24. TRI-STATE Output HIGH and LOW Enable and Disable Time

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