![Texas Instruments] **TEXAS INSTRUMENTS**

54ABT543

54ABT543 Octal Registered Transceiver with TRI-STATE® Outputs

Check for Samples: 54ABT543

FEATURES

- **Back-to-back registers for storage**
- **Bidirectional data path**
- **A and B outputs have current sourcing capability of 24 mA and current sinking capability of 48 mA**
- **Separate controls for data flow in each direction**
- **Guaranteed latchup protection**
- **High impedance glitch free bus loading during entire power up and power down cycle**
- **Nondestructive hot insertion capability**
- **Standard Military Drawing (SMD) 5962-9231401**

DESCRIPTION

The 'ABT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

Connection Diagram

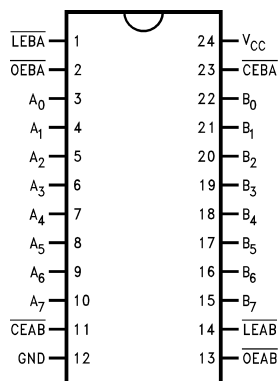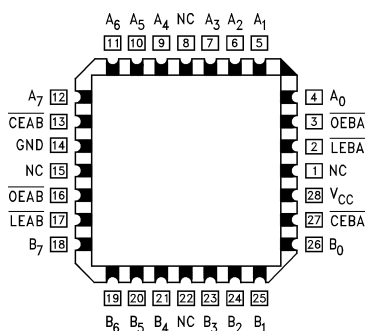**Figure 1. Pin Assignment for DIP and Flatpak**

Pin		Pin	
$\overline{LEBA}$	1	24	V_{CC}
$\overline{OEBA}$	2	23	$\overline{CEBA}$
A_0	3	22	B_0
A_1	4	21	B_1
A_2	5	20	B_2
A_3	6	19	B_3
A_4	7	18	B_4
A_5	8	17	B_5
A_6	9	16	B_6
A_7	10	15	B_7
$\overline{CEAB}$	11	14	$\overline{LEAB}$
GND	12	13	$\overline{OEAB}$

Figure 2. Pin Assignment for LCC

Top: A_6 (11), A_5 (10), A_4 (9), NC (8), A_3 (7), A_2 (6), A_1 (5)

Left: A_7 [12], $\overline{CEAB}$ [13], GND [14], NC [15], $\overline{OEAB}$ [16], $\overline{LEAB}$ [17], B_7 [18]

Right: [4] A_0, [3] $\overline{OEBA}$, [2] $\overline{LEBA}$, [1] NC, [28] V_{CC}, [27] $\overline{CEBA}$, [26] B_0

Bottom: [19] B_6, [20] B_5, [21] B_4, [22] NC, [23] B_3, [24] B_2, [25] B_1

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Pin Functions

Pin Descriptions

| Pin Names	Description
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable Inputs
$\overline{LEAB}$, $\overline{LEBA}$	Latch Enable Inputs
$\overline{CEAB}$, $\overline{CEBA}$	Chip Enable Inputs
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Functional Description

The 'ABT543 contains two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable ($\overline{CEAB}$) input must be low in order to enter data from the A port or take data from the B port as indicated in the Data I/O Control Table. With $\overline{CEAB}$ low, a low signal on ($\overline{LEAB}$) input makes the A to B latches transparent; a subsequent low to high transition of the $\overline{LEAB}$ line puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

Table 1. Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

Logic Diagram
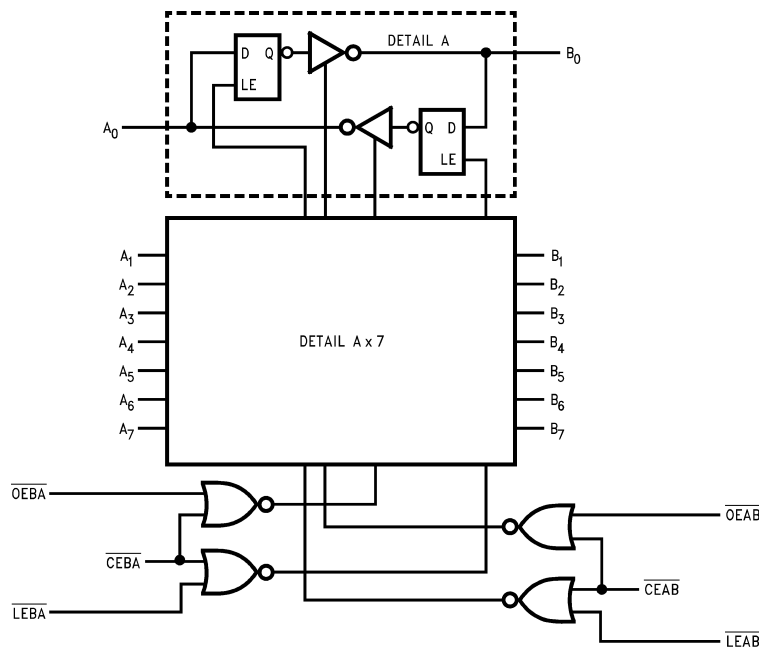
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [(1)]

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage [(2)]	−0.5V to +7.0V
Input Current [(2)]	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

(1) Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
(2) Either voltage limit or current limit is sufficient to protect inputs.

Recommended OperatingConditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

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DC Electrical Characteristics

Symbol	Parameter		ABT543			Units	V$_{CC}$	Conditions
			Min	Typ	Max			
V$_{IH}$	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V$_{IL}$	Input LOW Voltage				0.8	V		Recognized LOW Signal
V$_{CD}$	Input Clamp Diode Voltage				−1.2	V	Min	I$_{IN}$ = −18 mA (Non I/O Pins)
V$_{OH}$	Output HIGH Voltage	54ABT	2.5					I$_{OH}$ = −3 mA, (A$_n$, B$_n$)
		54ABT	2.0			V	Min	I$_{OH}$ = −24 mA, (A$_n$, B$_n$)
V$_{OL}$	Output LOW Voltage	54ABT			0.55	V	Min	I$_{OL}$ = 48 mA, (A$_n$, B$_n$)
V$_{ID}$	Input Leakage Test		4.75			V	0.0	I$_{ID}$ = 1.9 µA, (Non-I/O Pins)
								All Other Pins Grounded
I$_{IH}$	Input HIGH Current				5	µA	Max	V$_{IN}$ = 2.7V (Non-I/O Pins) [1]
								V$_{IN}$ = V$_{CC}$ (Non-I/O Pins)
I$_{BVI}$	Input HIGH Current Breakdown Test				7	µA	Max	V$_{IN}$ = 7.0V (Non-I/O Pins)
I$_{BVIT}$	Input HIGH Current				100	µA	Max	V$_{IN}$ = 5.5V (A$_n$, B$_n$)
	Breakdown Test (I/O)							
I$_{IL}$	Input LOW Current				−5	µA	Max	V$_{IN}$ = 0.5V (Non-I/O Pins) [1]
								V$_{IN}$ = 0.0V (Non-I/O Pins)
I$_{IH}$ + I$_{OZH}$	Output Leakage Current				50	µA	0V–5.5V	V$_{OUT}$ = 2.7V (A$_n$, B$_n$);
								$\overline{OEAB}$ or $\overline{CEAB}$ = 2V
I$_{IL}$ + I$_{OZL}$	Output Leakage Current				−50	µA	0V–5.5V	V$_{OUT}$ = 0.5V (A$_n$, B$_n$);
								$\overline{OEAB}$ or $\overline{CEAB}$ = 2V
I$_{OS}$	Output Short-Circuit Current		−100		−275	mA	Max	V$_{OUT}$ = 0V (A$_n$, B$_n$)
I$_{CEX}$	Output HIGH Leakage Current				50	µA	Max	V$_{OUT}$ = V$_{CC}$ (A$_n$, B$_n$)
I$_{ZZ}$	Bus Drainage Test				100	µA	0.0V	V$_{OUT}$ = 5.5V (A$_n$, B$_n$);
								All Others GND
I$_{CCLH}$	Power Supply Current				50	µA	Max	All Outputs HIGH
I$_{CCL}$	Power Supply Current				30	mA	Max	All Outputs LOW
I$_{CCZ}$	Power Supply Current				50	µA	Max	Outputs TRI-STATE
								All Others at V$_{CC}$ or GND
I$_{CCT}$	Additional I$_{CC}$/Input				2.5	mA	Max	V$_I$ = V$_{CC}$ − 2.1V
								All Others at V$_{CC}$ or GND
I$_{CCD}$	Dynamic I$_{CC}$	No Load						Outputs Open, $\overline{CEAB}$
	[1]				0.18	mA/MHz	Max	and $\overline{OEAB}$ = GND, $\overline{CEBA}$ = V$_{CC}$, One Bit Toggling,
								50% Duty Cycle, [2]

(1) Guaranteed but not tested.
(2) For 8-bit toggling. I$_{CCD}$ < 1.4 mA/MHz.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V$_{CC}$	Conditions C$_L$ = 50 pF, R$_L$ = 500Ω
V$_{OLP}$	Quiet Output Maximum Dynamic V$_{OL}$		1.1	V	5.0	T$_A$ = 25°C [1]
V$_{OLV}$	Quiet Output Minimum Dynamic V$_{OL}$		-0.45	V	5.0	T$_A$ = 25°C [1]

(1) Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW.

AC Electrical Characteristics

Symbol	Parameter	54ABT T_A = −55°C to +125°C V_{CC} = 4.5V–5.5V C_L = 50 pF		Units	Fig. No.
		Min	Max		
t_{PLH}	Propagation Delay	1.6	6.4	ns	Figure 4
t_{PHL}	A_n to B_n or B_n to A_n	1.6	6.2		
t_{PLH}	Propagation Delay				
t_{PHL}	$\overline{LEAB}$ to B_n, $\overline{LEBA}$ to A_n	1.6	6.6	ns	Figure 4
	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.6	6.4		
t_{PZH}	Enable Time				
t_{PZL}	$\overline{LEAB}$ to B_n, $\overline{LEBA}$ to A_n	1.3	6.4	ns	Figure 6
	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.8	7.4		
t_{PHZ}	Disable Time	2.0	7.2	ns	Figure 6
t_{PLZ}	$\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.5	7.0		

AC Operating Requirements

Symbol	Parameter	54ABT $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF		Units	Fig. No.
		Min	Max		
$t_S(H)$	Setup Time, HIGH or LOW	3.5		ns	Figure 7
$t_S(L)$	A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	3.0			
$t_H(H)$	Hold Time, HIGH or LOW	2.0		ns	Figure 7
$t_H(L)$	A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	2.0			
$t_S(H)$	Setup Time, HIGH or LOW	3.3		ns	Figure 7
$t_S(L)$	A_n or B_n to $\overline{CEAB}$ or $\overline{CEBA}$	2.5			
$t_H(H)$	Hold Time, HIGH or LOW	2.0		ns	Figure 7
$t_H(L)$	A_n or B_n to $\overline{CEAB}$ or $\overline{CEBA}$	2.0			
$t_W(L)$	Pulse Width, LOW	3.5		ns	Figure 5

Capacitance

Symbol	Parameter	Typ	Units	Conditions: $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$ (non I/O pins)
$C_{I/O}$[1]	Output Capacitance	11.0	pF	$V_{CC} = 5.0V$ (A_n, B_n)

(1) $C_{I/O}$ is measured at frequency, f = 1 MHz, PER MIL-STD-883, METHOD 3012.

AC Loading

*Includes jig and probe capacitance

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Figure 3. V_M = 1.5V
Input Pulse Requirements

Test Input Signal Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3V	1 MHz	500 ns	2.5 ns	2.5 ns
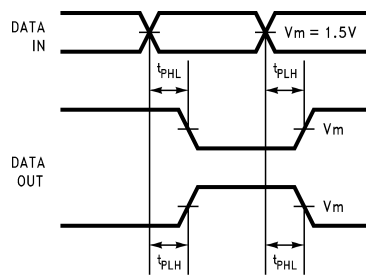
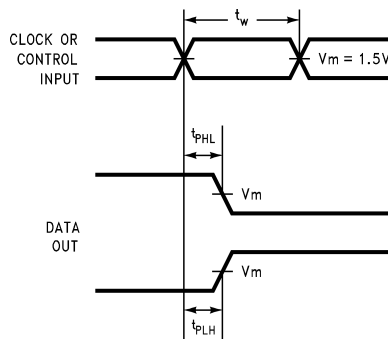**Figure 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**

Figure 5. Propagation Delay,
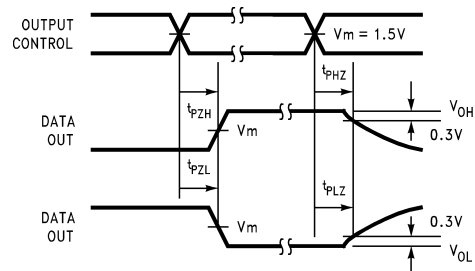**Pulse Width Waveforms**

**Figure 6. TRI-STATE Output HIGH
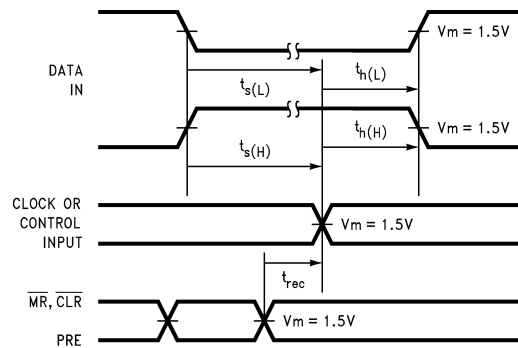and LOW Enable and Disable Times**

**Figure 7. Setup Time, Hold Time
and Recovery Time Waveforms**

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