National Semiconductor

July 1998

54ABT646
Octal Transceivers and Registers with TRI-STATE® Outputs

General Description

The 'ABT646 consists of bus transceiver circuits with TRI-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{OE}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{OE}$ is Active LOW. In the isolation mode (control $\overline{OE}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- A and B output sink capability of 48 mA, source capability of 24 mA
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9457701

Ordering Code

Military	Package Number	Package Description
54ABT646J-QML	J24A	24-Lead Ceramic Dual-In-Line
54ABT646W-QML	W24C	24-Lead Cerpack
54ABT646E-QML	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C

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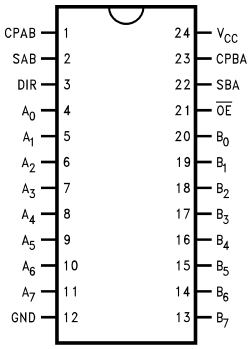
Connection Diagrams

Pin Assignment for DIP and Flatpak



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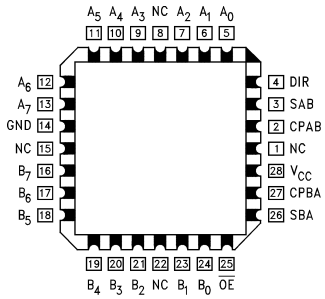
Pin Assignment for LCC



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Pin Descriptions

Pin Names	Description
A_0–A_7	Data Register A Inputs/ TRI-STATE Outputs
B_0–B_7	Data Register B Inputs/ TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
$\overline{OE}$	Output Enable Input
DIR	Direction Control Input

Connection Diagrams (Continued)

Real Time Transfer A-Bus to B-Bus

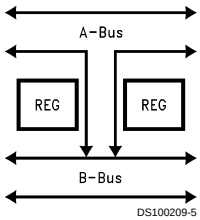


FIGURE 1.

Real Time Transfer B-Bus to A-Bus

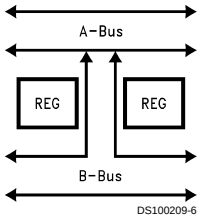


FIGURE 2.

Storage from Bus to Register

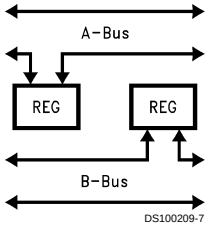


FIGURE 3.

Transfer from Register to Bus

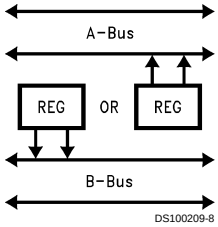


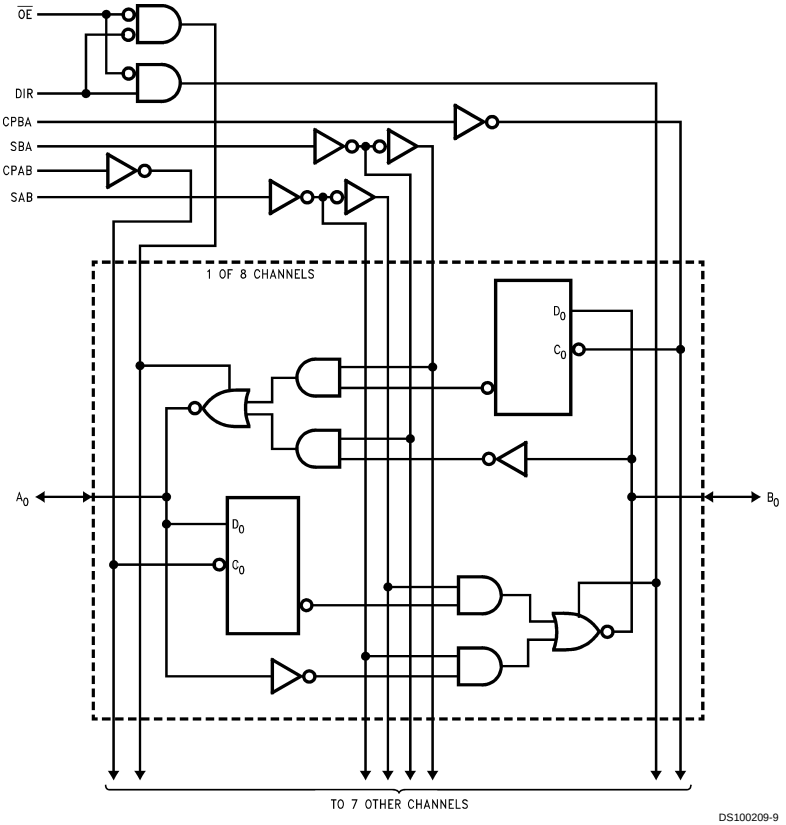
FIGURE 4.

Inputs						Data I/O (Note 1)		Function
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X			Isolation
H	X	↑	X	X	X	Input	Input	Clock A_n Data into A Register
H	X	X	↑	X	X			Clock B_n Data into B Register
L	H	X	X	L	X			A_n to B_n — Real Time (Transparent Mode)
L	H	↑	X	L	X	Input	Output	Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↑	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L			B_n to A_n — Real Time (Transparent Mode)
L	L	X	↑	X	L	Output	Input	Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↑	X	H			Clock B_n Data into B Register and Output to A_n

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition

Note 1: The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	ABT646 Min	ABT646 Typ	ABT646 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage 54ABT	2.5			V		I_{OH} = −3 mA, (A_n, B_n)
	54ABT	2.0				Min	I_{OH} = −24 mA, (A_n, B_n)
V_{OL}	Output LOW Voltage 54ABT			0.55	V	Min	I_{OL} = 48 mA, (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			5	µA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 5)
				5			V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	µA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	µA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−5	µA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 5)
				−5			V_{IN} = 0.0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			50	µA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current			−50	µA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	µA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			250	µA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			50	µA	Max	Outputs TRI-STATE; All Others GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V All Other Outputs at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 5)			0.18	mA/MHz	Max	Outputs Open $\overline{OE}$ and DIR = GND, Non-I/O = GND or V_{CC} (Note 4) One Bit toggling, 50% duty cycle

DC Electrical Characteristics (Continued)

Note 4: For 8-bit toggling, $I_{CCD} < 1.4$ mA/MHz.

Note 5: Guaranteed but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Max		
f_{max}	Max Clock Frequency	125		MHz	
t_{PLH}	Propagation Delay	2.2	8.8	ns	*Figure 8*
t_{PHL}	Clock to Bus	1.7	8.8		
t_{PLH}	Propagation Delay	1.5	7.9	ns	*Figure 8*
t_{PHL}	Bus to Bus	1.5	7.9		
t_{PLH}	Propagation Delay	1.5	8.1	ns	*Figure 8*
t_{PHL}	SBA or SAB to A_n to B_n	1.5	8.9		
t_{PZH}	Enable Time	1.0	7.3	ns	*Figure 10*
t_{PZL}	$\overline{OE}$ to A_n or B_n	1.9	8.8		
t_{PHZ}	Disable Time	1.5	9.3	ns	*Figure 10*
t_{PLZ}	$\overline{OE}$ to A_n or B_n	1.5	9.3		
t_{PZH}	Enable Time	1.0	7.7	ns	*Figure 10*
t_{PZL}	DIR to A_n or B_n	2.2	9.5		
t_{PHZ}	Disable Time	1.5	8.7	ns	*Figure 10*
t_{PLZ}	DIR to A_n or B_n	1.5	9.2		

AC Operating Requirements

Symbol	Parameter	54ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Max		
t_S(H) t_S(L)	Setup Time, HIGH or LOW Bus to Clock	3.5		ns	*Figure 11*
t_H(H) t_H(L)	Hold Time, HIGH or LOW Bus to Clock	1.0		ns	*Figure 11*
t_W(H) t_W(L)	Pulse Width, HIGH or LOW	4.0		ns	*Figure 9*

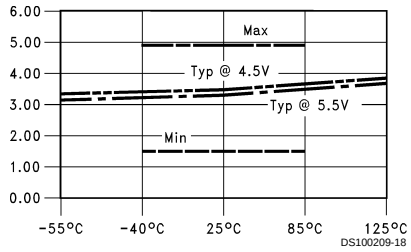
Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5	pF	V_{CC} = 0V (non I/O pins)
$C_{I/O}$ (Note 6)	Output Capacitance	11	pF	V_{CC} = 5.0V (A_n, B_n)

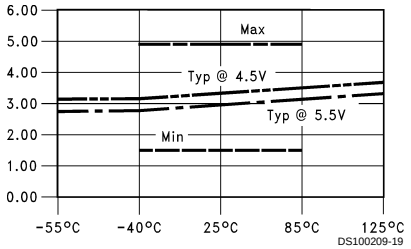
Note 6: $C_{I/O}$ is measured at frequency, f = 1 MHz, per MIL-STD-883B, Method 3012.

Capacitance (Continued)

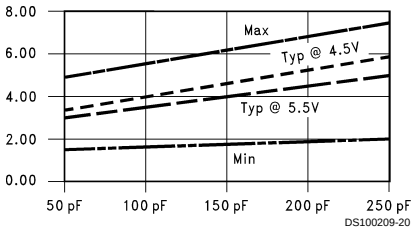
t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Clock to Bus



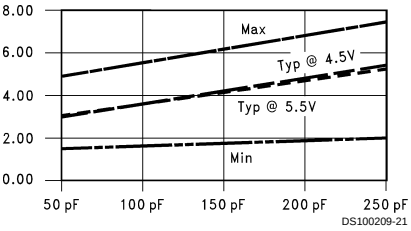
t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Clock to Bus



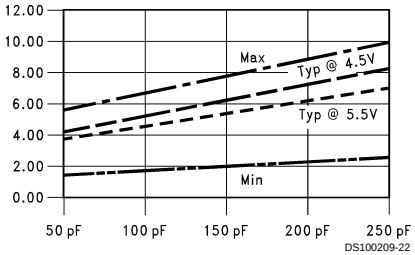
t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25˚C
Clock to Bus



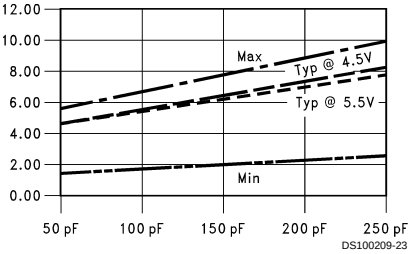
t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25˚C
Clock to Bus



t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25˚C
Clock to Bus



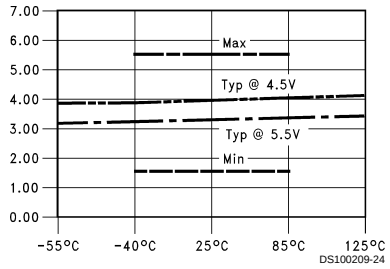
t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25˚C
Clock to Bus



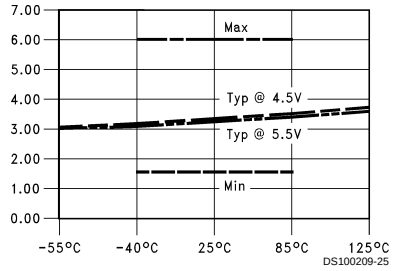
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

Capacitance (Continued)

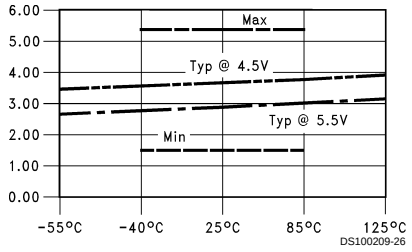
t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
OE to Bus



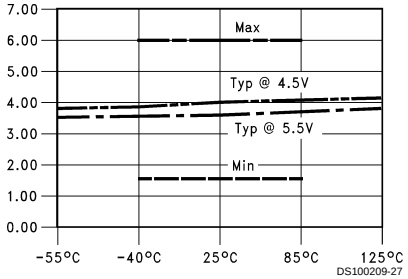
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
OE to Bus



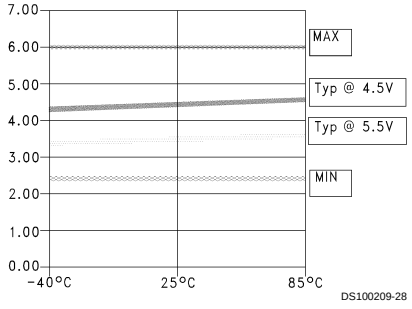
t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



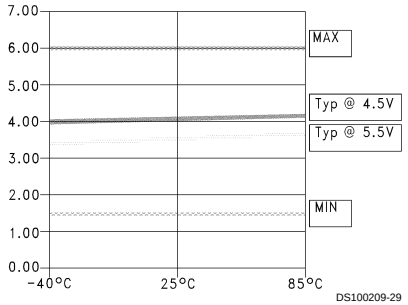
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
OE to Bus



t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching
OE to Bus



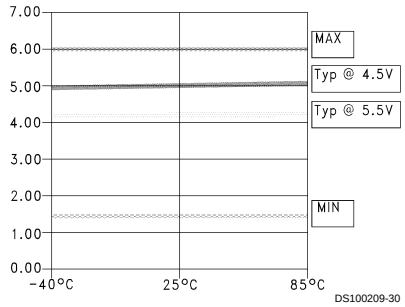
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching
OE to Bus



Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

Capacitance (Continued)

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching
OE to Bus



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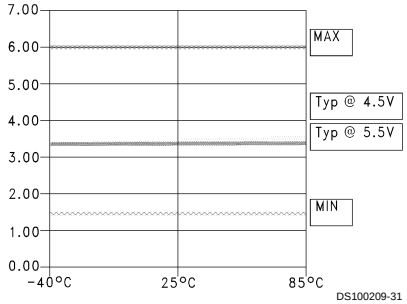
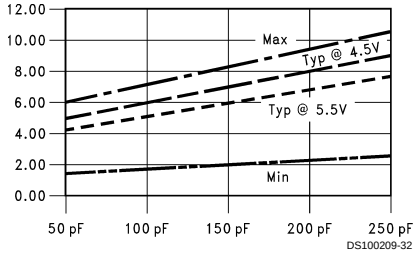
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching
OE to Bus



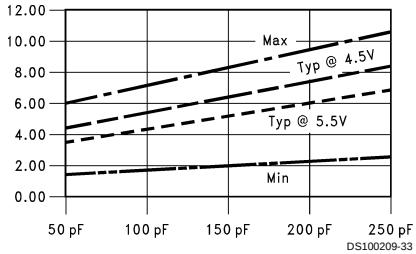
DS100209-31

t_{PZL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
OE to Bus



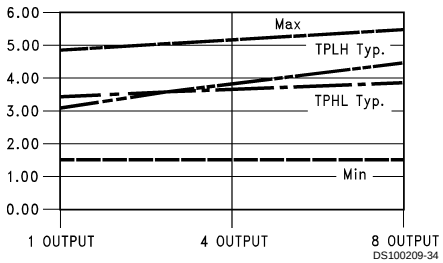
DS100209-32

t_{PZH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
OE to Bus



DS100209-33

t_{PLH} and t_{PHL} vs Number Output Switching
V_{CC} = 5.0V, T_A = 25°C
C_L = 50 pF, Clock to Bus



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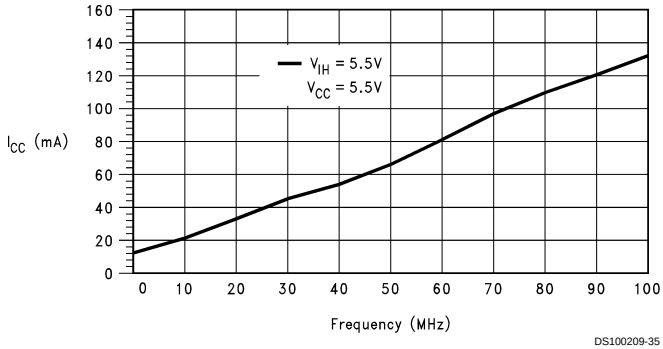
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

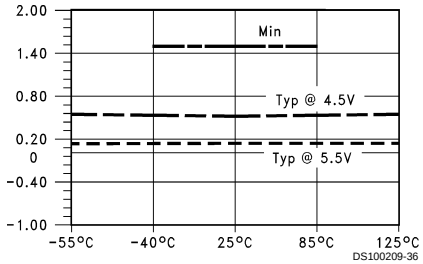
Capacitance (Continued)

I_{CC} vs Frequency, Average,
T_A = 25˚C, V_{CC} = 5.5V
All Outputs Unloaded/Unterminated;
All Outputs Switching in phase @50% Duty Cycle



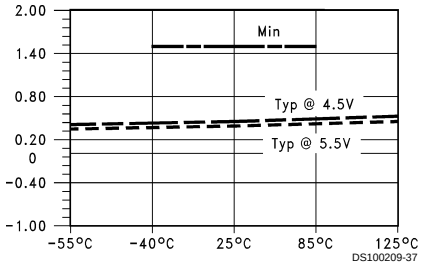
DS100209-35

t_{SET} LOW vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Clock



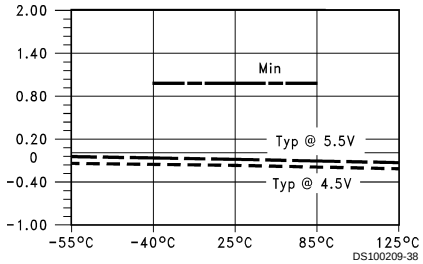
DS100209-36

t_{SET} HIGH vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Clock



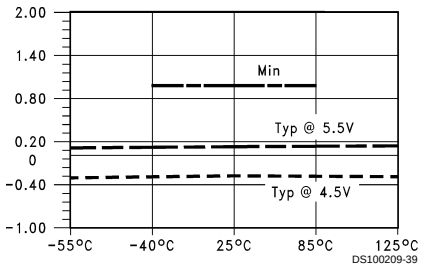
DS100209-37

t_{HOLD} LOW vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Clock



DS100209-38

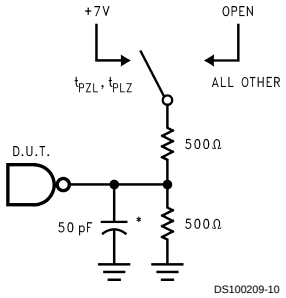
t_{HOLD} HIGH vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Clock



DS100209-39

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

AC Loading



*Includes jig and probe capacitance

FIGURE 5. Standard AC Test Load

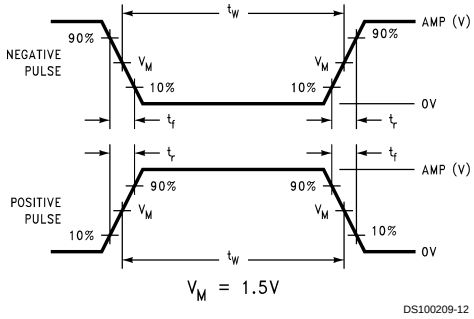


FIGURE 6. Test Input Signal Levels Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 7. Test Input Signal Requirements

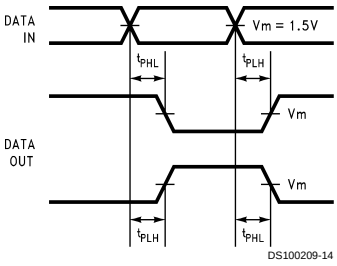


FIGURE 8. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

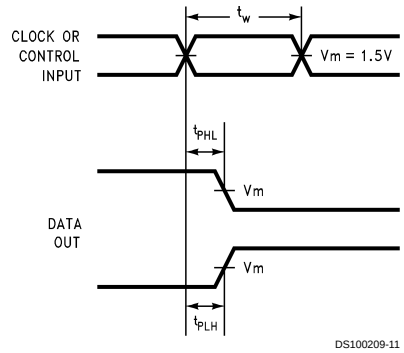


FIGURE 9. Propagation Delay, Pulse Width Waveforms

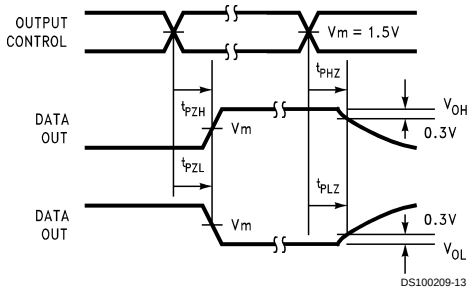


FIGURE 10. TRI-STATE Output HIGH and LOW Enable and Disable Times

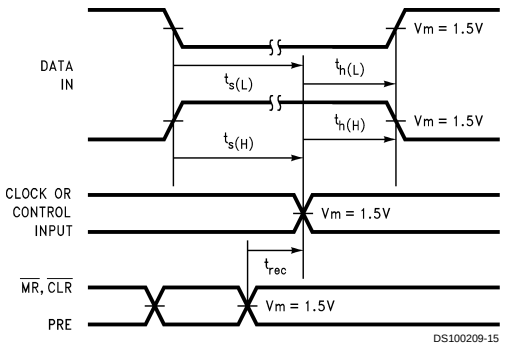
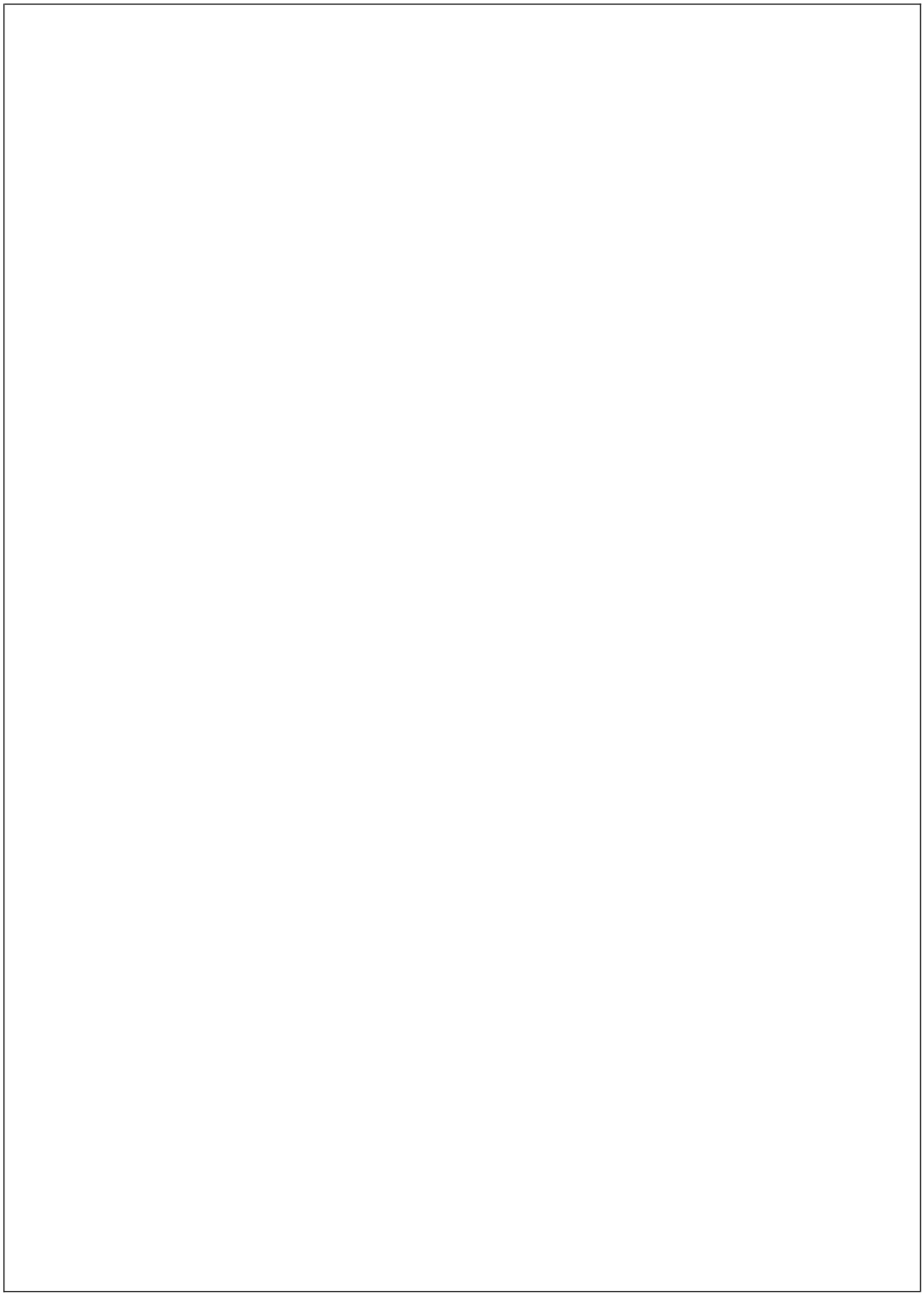
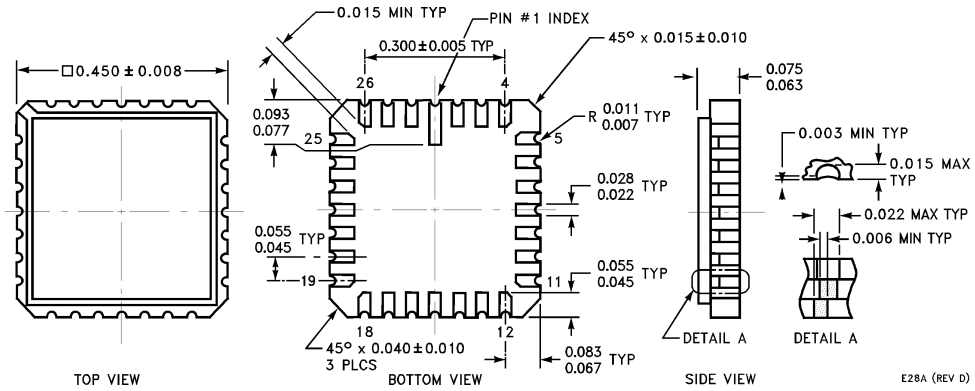


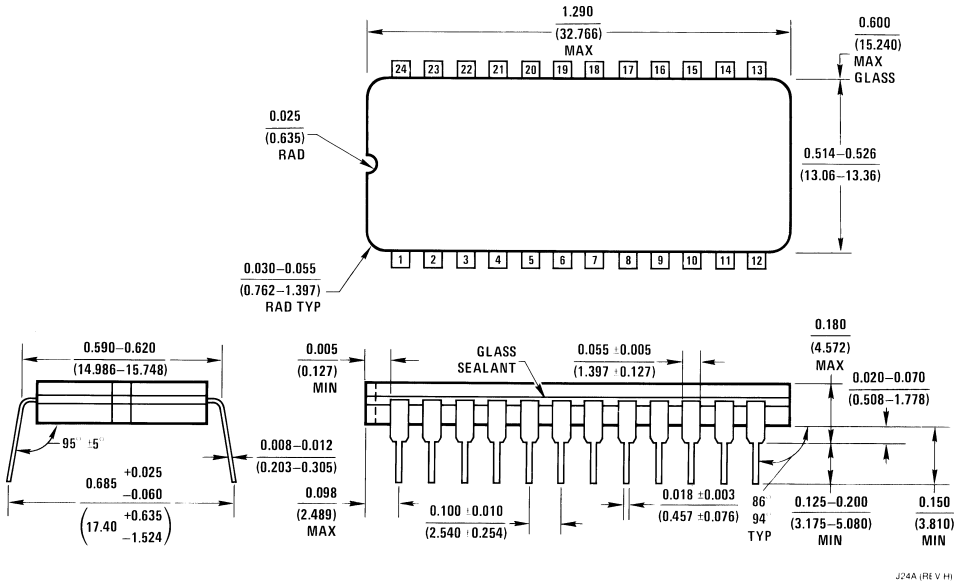
FIGURE 11. Setup Time, Hold Time and Recovery Time Waveforms



Physical Dimensions inches (millimeters) unless otherwise noted

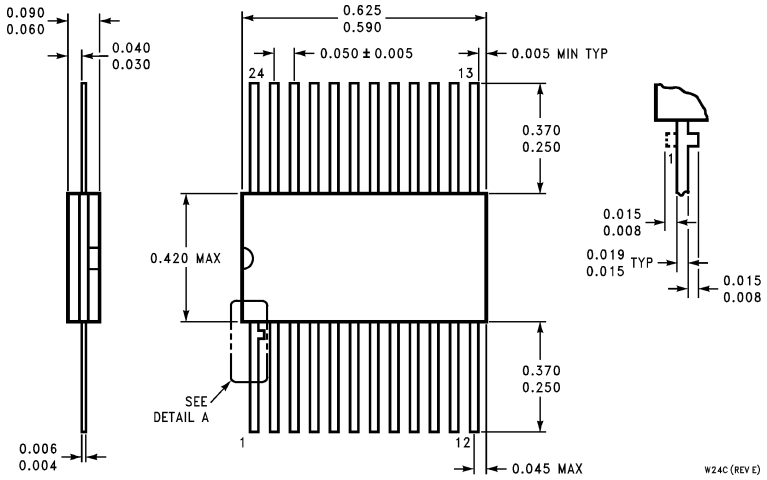


28-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E28A



24-Lead Ceramic Dual-in-Line Package (D)
NS Package Number J24A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Ceramic Flatpak Package (F)
NS Package Number W24C

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