

## 54AC257 • 54ACT257 Quad 2-Input Multiplexer with TRI-STATE® Outputs

Check for Samples: [54AC257](#), [54ACT257](#)

### FEATURES

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Multiplexer expansion by tying outputs together
- Noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT257 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC257: 5962-88703
  - 'ACT257: 5962-89689

### DESCRIPTION

The 'AC/'ACT257 is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (noninverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the common Output Enable ( $\overline{OE}$ ) input, allowing the outputs to interface directly with bus-oriented systems.

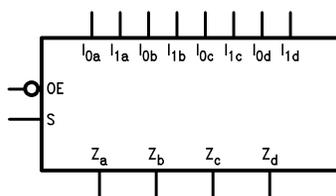
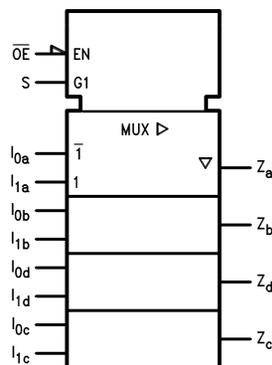


Figure 1. IEEE/IEC



Pin Names	Description
S	Common Data Select Input
$\overline{OE}$	TRI-STATE Output Enable Input
$I_{0a}$ – $I_{0d}$	Data Inputs from Source 0
$I_{1a}$ – $I_{1d}$	Data Inputs from Source 1
$Z_a$ – $Z_d$	TRI-STATE Multiplexer Outputs



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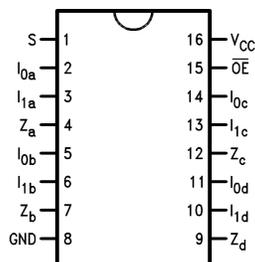
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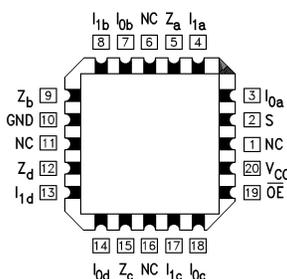
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## Connection Diagram

**Figure 2. Pin Assignment for DIP and Flatpak**



**Figure 3. Pin Assignment for LCC**



## Functional Description

The 'AC/ACT257 is quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the  $I_{0x}$  inputs are selected and when Select is HIGH, the  $I_{1x}$  inputs are selected. The data on the selected inputs appears at the outputs in true (noninverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = nOE \cdot (1_{1a} \cdot S + I_{0a} \cdot nS) \quad (1)$$

$$Z_b = nOE \cdot (1_{1b} \cdot S + I_{0b} \cdot nS) \quad (2)$$

$$Z_c = nOE \cdot (1_{1c} \cdot S + I_{0c} \cdot nS) \quad (3)$$

$$Z_d = nOE \cdot (1_{1d} \cdot S + I_{0d} \cdot nS) \quad (4)$$

When the Output Enable ( $\overline{OE}$ ) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

**Truth Table**  
(1)

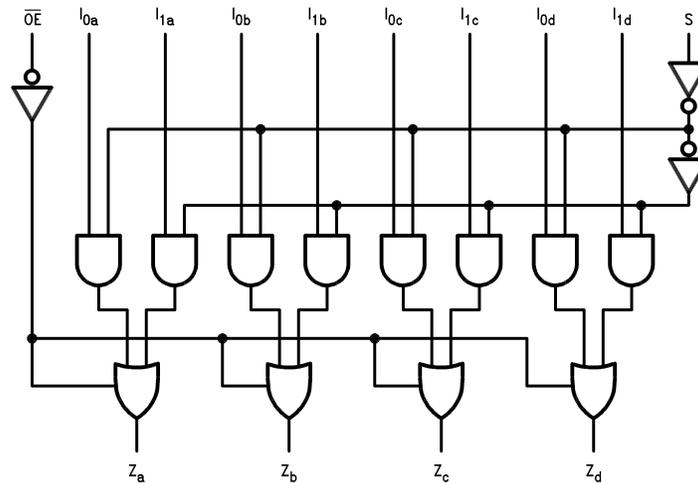
Output	Select	Data		Outputs
Enable	Input	Inputs		
$\overline{OE}$	S	$I_0$	$I_1$	Z
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H

- (1) H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

**Truth Table**  
(1) (continued)

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	$I_0$	$I_1$	Z
L	L	L	X	L
L	L	H	X	H

**Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings** (1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current	
( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current	
Per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
CDIP	175°C

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

### Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'AC Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

### DC Characteristics for 'AC Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	54AC		Units	Conditions	
			T <sub>A</sub> = -55°C to +125°C Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	2.1			V <sub>OUT</sub> = 0.1V	
		4.5	3.15	V		or V <sub>CC</sub> - 0.1V	
		5.5	3.85				
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	0.9			V <sub>OUT</sub> = 0.1V	
		4.5	1.35	V		or V <sub>CC</sub> - 0.1V	
		5.5	1.65				
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.9			I <sub>OUT</sub> = -50 μA	
		4.5	4.4	V			
		5.5	5.4				
						(1)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>
		3.0	2.4				-12 mA
		4.5	3.7	V		I <sub>OH</sub>	-24 mA
		5.5	4.7				-24 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.1			I <sub>OUT</sub> = 50 μA	
		4.5	0.1	V			
		5.5	0.1				
						(1)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>
		3.0	0.50				12 mA
		4.5	0.50	V		I <sub>OL</sub>	24 mA
		5.5	0.50				24 mA
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	±1.0	μA		V <sub>I</sub> = V <sub>CC</sub> , GND	
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	5.5	±10.0	μA		V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND	
I <sub>OLD</sub>	<sup>(2)</sup> Minimum Dynamic Output Current	5.5	50	mA		V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>		5.5	-50	mA		V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0	μA		V <sub>IN</sub> = V <sub>CC</sub> or GND	

(1) All outputs loaded; thresholds on input associated with output under test.

(2) Maximum test duration 2.0 ms, one output loaded at a time.

## DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	54ACT T <sub>A</sub> = -55°C to +125°C Guaranteed Limits	Units	Conditions	
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	2.0			
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	0.8			
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.4	V	I <sub>OUT</sub> = -50 μA	
		5.5	5.4			
					(1)	
					V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	
		4.5	3.70	V	I <sub>OH</sub>	-24 mA
		5.5	4.70			-24 mA
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.1	V	I <sub>OUT</sub> = 50 μA	
		5.5	0.1			
					(1)	
					V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	
		4.5	0.50	V	I <sub>OL</sub>	24 mA
		5.5	0.50			24 mA
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	5.5	±10.0	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND	
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	1.6	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	
I <sub>OLD</sub>	(2)Minimum	5.5	50	mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>	Dynamic Output Current	5.5	-50	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

(1) All outputs loaded; thresholds on input associated with output under test.

(2) Maximum test duration 2.0 ms, one output loaded at a time.

**AC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(1)</sup>		54AC T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		Units
		3.3	5.0	1.0	11.0	
t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	3.3	5.0	1.0	8.0	ns
		5.0	5.0	1.0	8.0	
t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	3.3	5.0	1.0	11.0	ns
		5.0	5.0	1.0	8.5	
t <sub>PLH</sub>	Propagation Delay S to Z <sub>n</sub>	3.3	5.0	1.0	14.5	ns
		5.0	5.0	1.0	11.0	
t <sub>PHL</sub>	Propagation Delay S to Z <sub>n</sub>	3.3	5.0	1.0	14.5	ns
		5.0	5.0	1.0	11.0	
t <sub>PZH</sub>	Output Enable Time	3.3	5.0	1.0	13.0	ns
		5.0	5.0	1.0	10.0	
t <sub>PZL</sub>	Output Enable Time	3.3	5.0	1.0	11.0	ns
		5.0	5.0	1.0	9.5	
t <sub>PHZ</sub>	Output Disable Time	3.3	5.0	1.0	13.0	ns
		5.0	5.0	1.0	11.0	
t <sub>PLZ</sub>	Output Disable Time	3.3	5.0	1.0	10.5	ns
		5.0	5.0	1.0	9.5	

(1) Voltage Range 3.3 is 3.0V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

**AC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(1)</sup>	54ACT T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		Units
t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	5.0	1.0	8.0	ns
t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	5.0	1.0	9.5	ns
t <sub>PLH</sub>	Propagation Delay S to Z <sub>n</sub>	5.0	1.0	11.0	ns
t <sub>PHL</sub>	Propagation Delay S to Z <sub>n</sub>	5.0	1.0	11.5	ns
t <sub>PZH</sub>	Output Enable Time	5.0	1.0	9.5	ns
t <sub>PZL</sub>	Output Enable Time	5.0	1.0	9.5	ns
t <sub>PHZ</sub>	Output Disable Time	5.0	1.0	10.5	ns
t <sub>PLZ</sub>	Output Disable Time	5.0	1.0	9.5	ns

(1) Voltage Range 5.0 is 5.0V ±0.5V

**Capacitance**

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = OPEN$
$C_{PD}$	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.0V$

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