54AC74/54ACT74 Dual D-Type Positive Edge-Triggered Flip-Flop

Check for Samples: 54AC74, 54ACT74

FEATURES

- **I_{CC} reduced by 50%**
- **Output source/sink 24 mA**
- **'ACT74 has TTL-compatible inputs**
- **Standard Microcircuit Drawing (SMD)**
  - **'AC74: 5962-88520**
  - **'ACT74: 5962-87525**
- **54AC74 now qualified to 300Krad RHA designation, refer to the SMD for more information**

DESCRIPTION

The 'AC/'ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level

LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

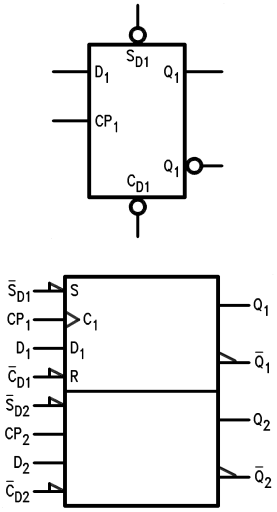
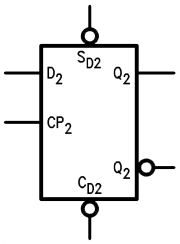


Figure 1. IEEE/IEC



Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

Connection Diagram

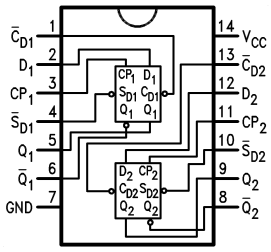


Figure 2. Pin Assignment for DIP and Flatpak

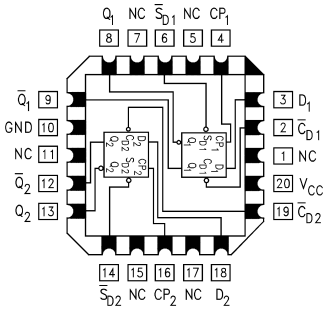


Figure 3. Pin Assignment for LCC

Truth Table
(1)

(Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

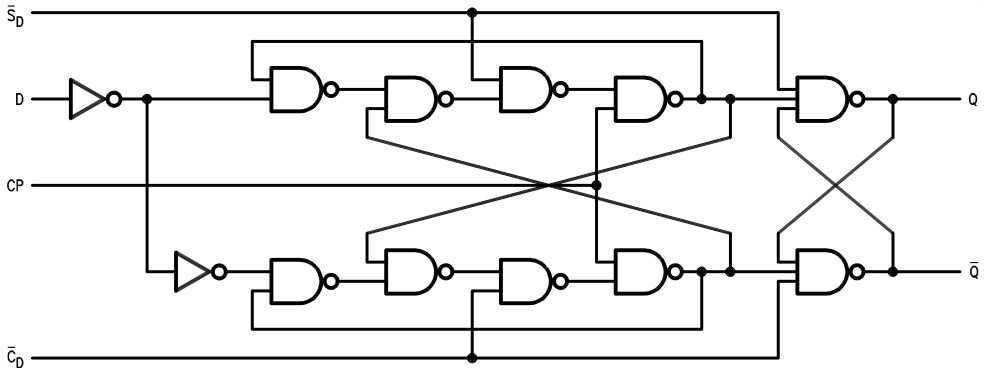
(1) H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
= LOW-to-HIGH Clock Transition
$Q_0(\overline{Q}_0)$ = Previous $Q(\overline{Q})$ before LOW-to-HIGH Transition of Clock

Truth Table (1) (continued)

(Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
H	H		H	H	L
H	H		L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

Recommended OperatingConditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

			54AC		
Symbol	**Parameter**	**V_{CC}**	**T_A =**	**Units**	**Conditions**
		(V)	**−55°C to +125°C**		
			Guaranteed Limits		
V_{IH}	Minimum High	3.0	2.1		V_{OUT} = 0.1V
	Level Input	4.5	3.15	V	or V_{CC} − 0.1V
	Voltage	5.5	3.85		
V_{IL}	Maximum Low	3.0	0.9		V_{OUT} = 0.1V
	Level Input	4.5	1.35	V	or V_{CC} − 0.1V
	Voltage	5.5	1.65		
V_{OH}	Minimum High	3.0	2.9		I_{OUT} = −50 µA
	Level Output	4.5	4.4	V	
	Voltage	5.5	5.4		
					(1) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4		−12 mA
		4.5	3.7	V	I_{OH} −24 mA
		5.5	4.7		−24 mA
V_{OL}	Maximum Low	3.0	0.1		I_{OUT} = 50 µA
	Level Output	4.5	0.1	V	
	Voltage	5.5	0.1		
					(1) V_{IN} = V_{IL} or V_{IH}
		3.0	0.5		12 mA
		4.5	0.5	V	I_{OL} 24 mA
		5.5	0.5		24 mA
I_{IN}	Maximum Input	5.5	±1.0	µA	V_I = V_{CC}, GND
	Leakage Current				
I_{OLD}	(2)Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5	40.0	µA	V_{IN} = V_{CC}
	Supply Current				or GND

(1) All outputs loaded; thresholds on input associated with output under test.
(2) Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices

			54ACT		
Symbol	**Parameter**	**V_{CC}**	**T_A =**	**Units**	**Conditions**
		(V)	**−55°C to +125°C**		
			Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V_{OUT} = 0.1V
		5.5	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V_{OUT} = 0.1V
		5.5	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I_{OUT} = −50 µA
		5.5	5.4		
					(1) V_{IN} = V_{IL} or V_{IH}
		4.5	3.70	V	I_{OH} −24 mA
		5.5	4.70		−24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I_{OUT} = 50 µA
		5.5	0.1		
					(1) V_{IN} = V_{IL} or V_{IH}
		4.5	0.50	V	I_{OL} 24 mA
		5.5	0.50		24 mA
I_{IN}	Maximum Input	5.5	±1.0	µA	V_I = V_{CC}, GND
	Leakage Current				
I_{CCT}	Maximum	5.5	1.6	mA	V_I = V_{CC} − 2.1V
	I_{CC}/Input				
I_{OLD}	(2)Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5	40.0	µA	V_{IN} = V_{CC}
	Supply Current				or GND

(1) All outputs loaded; thresholds on input associated with output under test.
(2) Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

		V_{CC}	54AC			
Symbol	**Parameter**	**(V)**	**T_A = −55°C to +125°C**		**Units**	**Fig.**
		(1)	**C_L = 50 pF**			**No.**
			Min	**Max**		
f_{max}	Maximum Clock	3.3	70		MHz	
	Frequency	5.0	95			
t_{PLH}	Propagation Delay	3.3	1.0	13.0	ns	
	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	9.5		
t_{PHL}	Propagation Delay	3.3	1.0	14.0	ns	
	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	10.5		
t_{PLH}	Propagation Delay	3.3	1.0	17.5	ns	
	CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	12.0		
t_{PHL}	Propagation Delay	3.3	1.0	13.5	ns	
	CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	10.0		

(1) Voltage Range 3.3 is 3.3V ± 0.3V Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements

			54AC		
Symbol	**Parameter**	**V_{CC}**	**T_A = −55°C to +125°C**	**Units**	**Fig.**
		(V)	**C_L = 50 pF**		**No.**
		(1)	**Guaranteed Limits**		
t_s	Set-up Time, HIGH or LOW	3.3	5.0	ns	
	D_n to CP_n	5.0	4.0		
t_h	Hold Time, HIGH or LOW	3.3	0.5	ns	
	D_n to CP_n	5.0	0.5		
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	3.3	8.0	ns	
	Pulse Width	5.0	5.5		
t_{rec}	Recovery Time	3.3	0.5	ns	
	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	0.5		

(1) Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

			54ACT			
		V_{CC}	T_A = −55°C			Fig.
Symbol	Parameter	(V)	to +125°C		Units	No.
		(1)	C_L = 50 pF			
			Min	Max		
f_{max}	Maximum Clock	5.0	85		MHz	
	Frequency					
t_{PLH}	Propagation Delay	5.0	1.0	11.5	ns	
	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$					
t_{PHL}	Propagation Delay	5.0	1.0	12.5	ns	
	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$					
t_{PLH}	Propagation Delay	5.0	1.0	14.0	ns	
	CP_n to Q_n or $\overline{Q}_n$					
t_{PHL}	Propagation Delay	5.0	1.0	12.0	ns	
	CP_n to Q_n or $\overline{Q}_n$					

(1) Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

			54ACT		
Symbol	**Parameter**	**V_{CC}**	**T_A = −55°C**	**Units**	**Fig.**
		(V)	**C_L = 50 pF**		**No.**
		(1)	**Guaranteed Limits**		
t_s	Set-up Time, HIGH or LOW	5.0	4.0	ns	
	D_n to CP_n				
t_h	Hold Time, HIGH or LOW	5.0	1.0	ns	
	D_n to CP_n				
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	5.0	7.0	ns	
	Pulse Width				
t_{rec}	Recovery Time	5.0	0.5	ns	
	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP				

(1) Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation	35.0	pF	V_{CC} = 5.0V
	Capacitance			

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