54ACT823 9-Bit D Flip-Flop

Check for Samples: 54ACT823

FEATURES

- **Outputs source/sink 24 mA**
- **TRI-STATE outputs for bus interfacing**
- **Inputs and outputs are on opposite sides**
- **ACT823 has TTL-compatible inputs**
- **Standard Microcircuit Drawing (SMD) 5962-9161001**

DESCRIPTION

The ACT823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The ACT823 offers noninverting outputs and is fully compatible with AMD's Am29823.

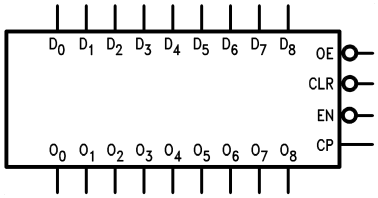
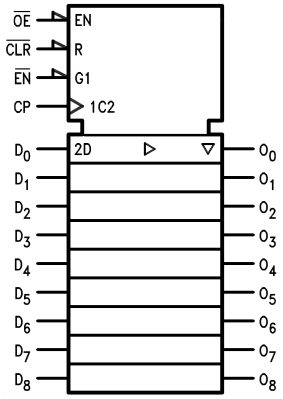


Figure 1. IEEE/IEC



Pin Names	Description
D_0–D_8	Data Inputs
O_0–O_8	Data Outputs
$\overline{OE}$	Output Enable
$\overline{CLR}$	Clear
CP	Clock Input
$\overline{EN}$	Clock Enable

Connection Diagram

Figure 2. Pin Assignment for DIP and Cerpack

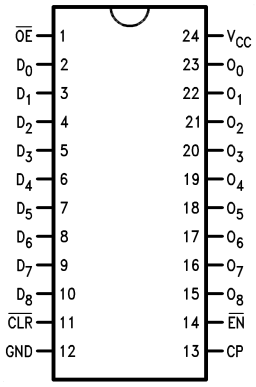
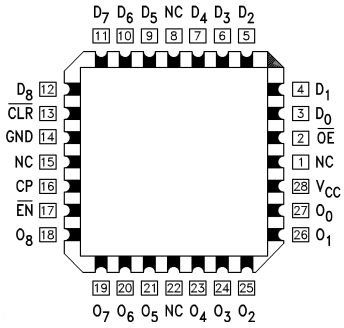


Figure 3. Pin Assignment for LCC



Functional Description

The ACT823 consists of nine D-type edge-triggered flip-flops. These have TRI-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}$ LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These devices are ideal for parity bus interfacing in high performance systems.

When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Table 1. Function Table(1)

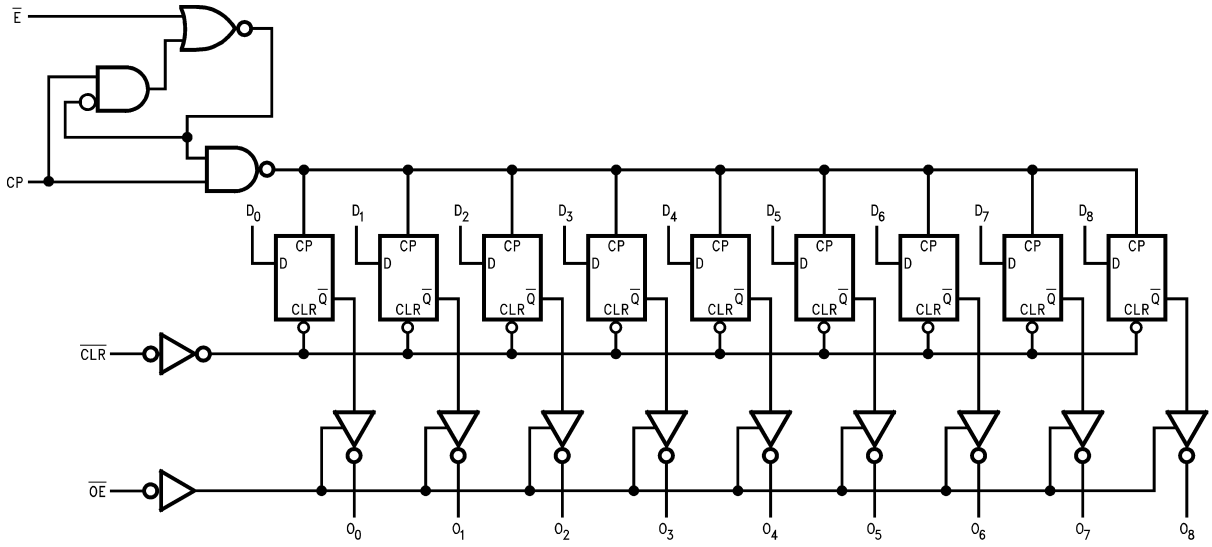
Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	Q	O	
H	X	L	N	L	L	Z	High Z

(1) H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
N = LOW-to-HIGH Transition
NC = No Change

Table 1. Function Table(1) (continued)

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	Q	O	
H	X	L	N	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	N	L	L	Z	Load
H	H	L	N	H	H	Z	Load
L	H	L	N	L	L	L	Load
L	H	L	N	H	H	H	Load

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current	
(I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics[1]

Symbol	Parameter	V_{CC}	T_A =	Units	Conditions
		(V)	−55°C to +125°C		
V_{IH}	Minimum High Level	4.5	2.0	V	V_{OUT} = 0.1V
	Input Voltage	5.5	2.0		or V_{CC} −0.1V
V_{IL}	Maximum Low Level	4.5	0.8	V	V_{OUT} = 0.1V
	Input Voltage	4.5	0.8		or V_{CC} −0.1V
V_{OH}	Minimum High Level Output Voltage	4.5	3.7	V	I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.5	V	I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE	5.5	±10.0	µA	V_I = V_{IL}, V_{IH}
	Current				V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} −2.1V
I_{OLD}	[2]Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5	160	µA	V_{IN} = V_{CC}
	Supply Current				or GND

(1) All outputs loaded; thresholds on input associated with output under test.
(2) Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (1)	T_A = −55°C to +125°C C_L = 50 pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Clock	5.0	95		MHz	
	Frequency					
t_{PLH}	Propagation Delay	5.0	1.0	12.0	ns	
	CP to O_n					
t_{PHL}	Propagation Delay	5.0	1.0	12.0	ns	
	CP to O_n					
t_{PHL}	Propagation Delay	5.0	1.0	18.0	ns	
	$\overline{CLR}$ to O_n					
t_{PZH}	Output Enable Time	5.0	1.0	11.5	ns	
	$\overline{OE}$ to O_n					
t_{PZL}	Output Enable Time	5.0	1.0	12.0	ns	
	$\overline{OE}$ to O_n					
t_{PHZ}	Output Disable Time	5.0	1.0	13.5	ns	
	$\overline{OE}$ to O_n					
t_{PLZ}	Output Disable Time	5.0	1.0	12.0	ns	
	$\overline{OE}$ to O_n					

(1) Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}(V) (1)	T_A = −55°C to +125°C C_L = 50 pF	Units	Fig.
			Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW	5.0	4.0	ns	
	D to CP				
t_h	Hold Time, HIGH or LOW	5.0	3.0	ns	
	D_n to CP				
t_s	Setup Time, HIGH or LOW	5.0	4.0	ns	
	$\overline{EN}$ to CP				
t_h	Hold Time, HIGH or LOW	5.0	3.0	ns	
	$\overline{EN}$ to CP				
t_w	CP Pulse Width	5.0	6.0	ns	
	HIGH or LOW				
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	7.5	ns	
t_{rec}	$\overline{CLR}$ to CP	5.0	4.5	ns	
	Recovery Time				

(1) Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	4.4	pF	V_{CC} = 5.0V

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