National Semiconductor

54ACT/74ACT825
8-Bit D Flip-Flop

General Description

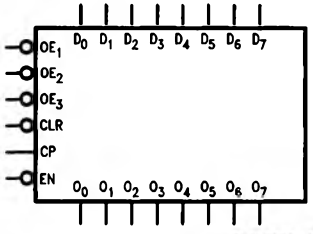
The 'ACT825 is an 8-bit buffered register. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multi-use control of the interface. The 'ACT825 has noninverting outputs and is fully compatible with AMD's Am29825.

Features

- Outputs source/sink 24 mA
- Inputs and outputs are on opposite sides
- 'ACT825 has TTL-compatible inputs

Ordering Code: See Section 8

Logic Symbols



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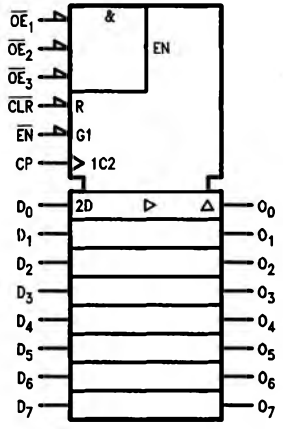
IEEE/IEC



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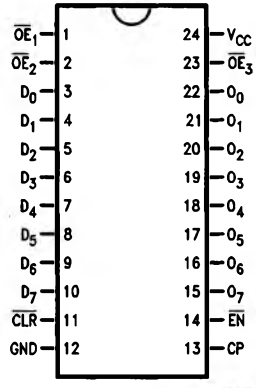
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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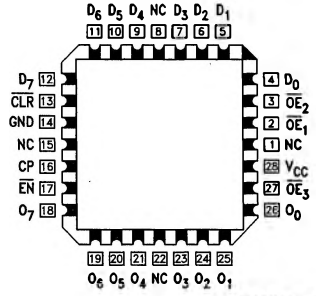
Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	Output Enables
$\overline{EN}$	Clock Enable
$\overline{CLR}$	Clear
CP	Clock Input

Pin Assignment for LCC



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Functional Description

The 'ACT825 consists of eight D-type edge-triggered flip-flops. These devices have TRI-STATE® outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}_1$, $\overline{OE}_2$ and $\overline{OE}_3$ LOW, the contents of the flip-flops are available at the outputs. When one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the outputs go to the high impedance state.

Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The 'ACT825 has Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These pins are ideal for parity bus interfacing in high performance systems.

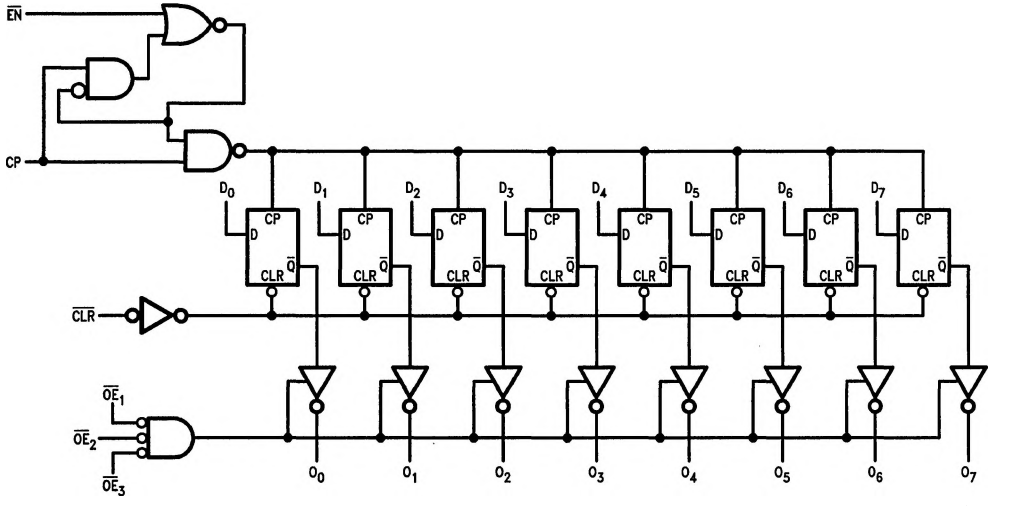
When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D_n	Q	O	
H	X	L	⌐	L	L	Z	High-Z
H	X	L	⌐	H	H	Z	High-Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	⌐	L	L	Z	Load
H	H	L	⌐	H	H	Z	Load
L	H	L	⌐	L	L	L	Load
L	H	L	⌐	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	+0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74ACT T_A = 25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8		V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} −2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	120	158		95		109		MHz	
t_{PLH}	Propagation Delay CP to O_n	5.0	1.5	5.5	9.5	1.0	11.5	1.5	10.5	ns	2–3, 4
t_{PHL}	Propagation Delay CP to O_n	5.0	2.0	5.5	9.5	1.0	11.5	1.5	10.5	ns	2–3, 4
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0	2.5	8.0	13.5	1.0	18.0	2.0	15.5	ns	2–3, 4
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	1.5	6.0	10.5	1.0	11.5	1.5	11.5	ns	2–5
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.0	6.5	11.0	1.0	12.5	1.5	12.0	ns	2–6
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	6.5	11.0	1.0	13.5	1.5	12.0	ns	2–5
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	6.0	10.5	1.0	13.0	1.5	11.5	ns	2–6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	0.5	2.5	4.0	2.5	ns	2–7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	2.5	3.0	2.5	ns	2–7
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	5.0	0	2.0	4.0	2.5	ns	2–7
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	5.0	0	1.0	3.0	1.0	ns	2–7
t_w	CP Pulse Width HIGH or LOW	5.0	2.5	4.5	6.0	5.5	ns	2–3
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	3.0	5.5	7.0	5.5	ns	2–3
t_{rec}	$\overline{CLR}$ to CP Recovery Time	5.0	1.5	3.5	4.5	4.0	ns	2–3, 7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	44	pF	$V_{CC} = 5.0V$