ADVANCE INFORMATION

National Semiconductor

54ACTQ/74ACTQ843 Quiet Series 8-Bit Transparent Latch

General Description

The 'ACTQ843 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths. The 'ACTQ843 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on oppostie sides of package for easy interface with microprocessors
- Improved latch-up immunity
- Outputs source/sink 24 mA
- ACTQ843 has TTL-compatible inputs
- Functionally and pin-compatible to AMD's AM29843
- 4 kV minimum ESD immunity
- 'ACT843 has TTL-compatible inputs
- TRI-STATE® outputs for bus interfacing

Logic Symbols Connection Diagrams Pin Assignment 1 ŌE -EN for DIP. Flatpak and SOIC Do D1 D2 D3 D4 D5 D6 D7 PRE . **S2** OE R 0 CIR ÕF 24 -V_{cc} CI LE LE 23 Do -00 2 D1 --01 PRE Do 1D ⊳ 27 00 3 22 0 01 0, 0, 0, 0, 05 06 0-٥, 01 Dţ D2 . A 21 ·02 D3. •03 D2 ٥, 5 20 TL/F/10689-1 03 D٦ 6 D4 19 •0, 04 •0₅ D, D₅ 7 18 D₅ 05 8 D₆ 17 -06 De 06 9 D7 . 16 -07 07 D-7 D₈ 10 15 08 D₈ 08 CLR 11 PRE 14 TI /F/10689-4 GND . 12 -1 F 13 TL/F/10689-2 **Pin Assignment** for LCC **Pin Names** Description D7 D6 D5 NC D4 D3 D2 D0-D7 Data Inputs 11098765 Data Outputs 00-07 ŌĒ **Output Enable** D₈ 12 ₫ D₁ Latch Enable LE CLR 13 S 00 CLR Clear GND 14 2 OE PRE Preset NC 15 1 NC 28 V_{CC} LE 16 PRE [7] 27 00 0, 18 26 01 19 20 21 22 23 24 25 07 06 05 NC 04 03 02 TL/F/10689-3

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