

54F/74F420

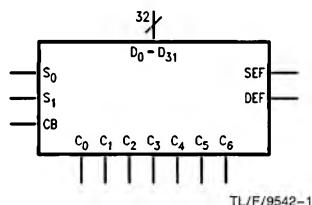
Parallel Check Bit/Syndrome Bit Generator

General Description

The 'F420 is a parallel check bit/syndrome bit generator. The 'F420 utilizes a modified hamming code to generate 7 check bits from a 32-bit dataword, in 15 ns, when operated in the check bit generate mode. When operated in the syndrome generate mode, the check bits and data bits

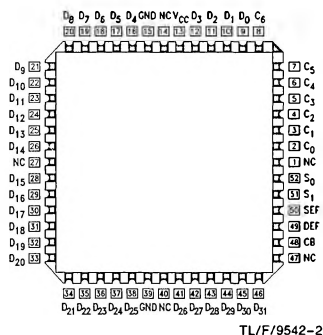
read from memory are utilized in a parity summer to generate syndrome bits upon error detection. The maximum error count detectable is 2. A single error detect can occur in 18 ns; a double error detect in 22 ns. The syndrome bit generation can be output in 15 ns (maximum).

Logic Diagram

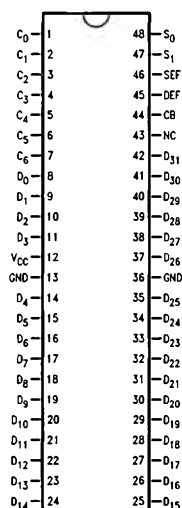


Connection Diagrams

Pin Assignment
for LCC and PCC



Pin Assignment
for DIP and Flatpak



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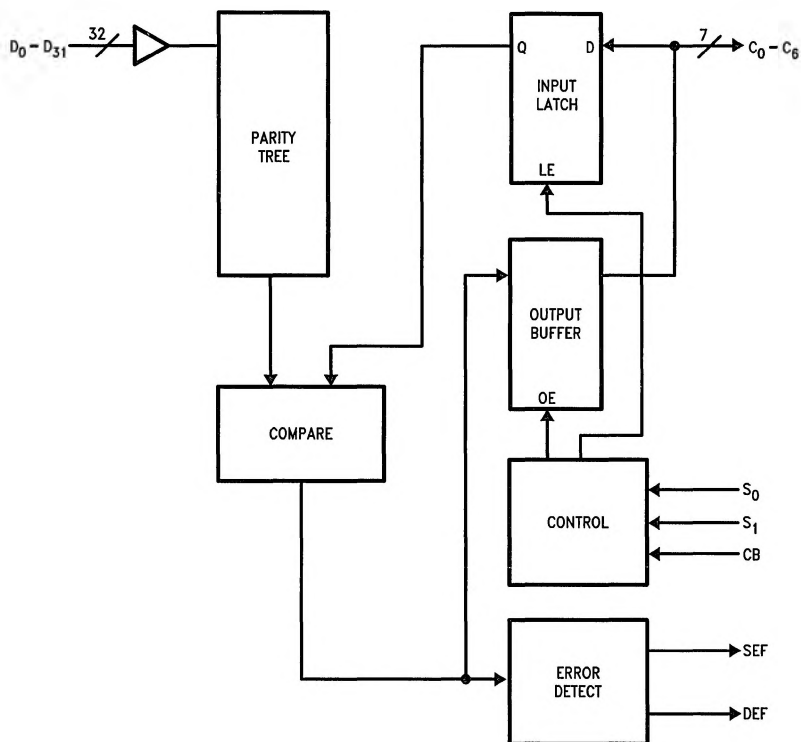
Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
C ₀ -C ₆	Check Bit/Syndrome Bus Inputs/ Outputs	3.5/1.083 150/40 (33.3)	70 μ A/ -0.65 mA -3 mA/24 mA (20 mA)
D ₀ -D ₃₁	Data Bit Bus	1.0/1.0	20 μ A/ -0.6 mA
CB	Check Bit Control	1.0/1.0	20 μ A/ -0.6 mA
DEF	Double Error Flag	50/33.3	-1 mA/20 mA
SEF	Single Error Flag	50/33.3	-1 mA/20 mA
S ₀ , S ₁	Mode Control	1.0/1.0	20 μ A/ -0.6 mA

Function Table

Memory Cycle	Function	Control		Check Bit	CB Control I/O	Error Flags	
		S ₁	S ₀			SEF	DEF
Write	Generate Check Bits	L	L	Output Check	L	H	H
Read	Read & Flag	H	L	Input	H	Enabled	
Read	Latch Check Bits	H	H	Inputs	H	Enabled	
Read	Output Syndrome Bits	H	H	Output Syndrome Bits	L	Enabled	
Diagnostics	Input Diagnostic	H	H	Latched Check	H	Enabled	
	Data Word			Outputs High-Z			
Diagnostics	Input Diagnostic	L	H	Output Latched	L	Enabled	
	Data Word			Check Bits			
Diagnostics	Input Diagnostic	H	H	Output Syndrome	L	Enabled	
	Data Word			Bits			

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA, D _n , CB, S ₀ , S ₁
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I _{OH} = −1 mA (All Outputs) I _{OH} = −3 mA (C ₀ –C ₆) I _{OH} = −1 mA (All Outputs) I _{OH} = −3 mA (C ₀ –C ₆) I _{OH} = −1 mA (All Outputs) I _{OH} = −3 mA (C ₀ –C ₆)
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC}		0.5 0.5 0.5	V	Min	I _{OL} = 20 mA (All Outputs) I _{OL} = 20 mA (DEF, SEF) I _{OL} = 24 mA (C ₀ –C ₆)
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 1.50 mV All Other Pins Grounded
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			1.0	mA	Max	V _{IN} = 5.5V (C ₀ –C ₆)
I _{IL}	Input LOW Current			−0.6	mA	Max	V _{IN} = 0.5V (D _n , CB, S ₀ , S ₁)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (C ₀ –C ₆)
I _{IL} + I _{OZL}	Output Leakage Current			−650	μA	Max	V _{OUT} = 0.5V (C ₀ –C ₆)
I _{OS}	Output Short-Circuit Current			−60	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCH}	Power Supply Current			130	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current			130	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current			130	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

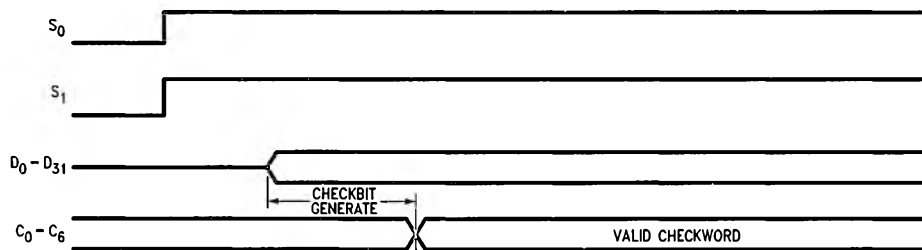
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay D_n to C_n	5.0		20.0			5.0	22.0	ns
		5.0		17.0			5.0	19.0	
t_{PLH} t_{PHL}	Propagation Delay D_n/C_n to SEF	5.0		20.0			5.0	22.0	ns
		4.0		16.0			4.0	18.0	
t_{PLH} t_{PHL}	Propagation Delay D_n/C_n to DEF	6.0		24.0			6.0	26.0	ns
		5.0		21.0			5.0	22.0	
t_{PLH} t_{PHL}	Propagation Delay S_1 to C_n	4.0		18.0			4.0	19.0	ns
		3.0		13.0			3.0	14.0	
t_{PLH} t_{PHL}	Propagation Delay S_1 to SEF/DEF	4.0		14.0			4.0	15.0	ns
		3.0		9.0			3.0	10.0	
t_{PZH} t_{PZL}	Output Enable Time	2.0		12.0			2.0	13.0	ns
		2.0		11.0			2.0	12.0	
t_{PHZ} t_{PLZ}	Output Disable Time	1.0		7.5			1.0	8.0	ns
		1.0		7.5			1.0	8.0	

AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW C_n to S_0	5.0 5.0				5.0 5.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW C_n to S_0	5.0 5.0				5.0 5.0		
$t_w(\text{L})$	Clock Pulse Width LOW	8.0				8.0		ns

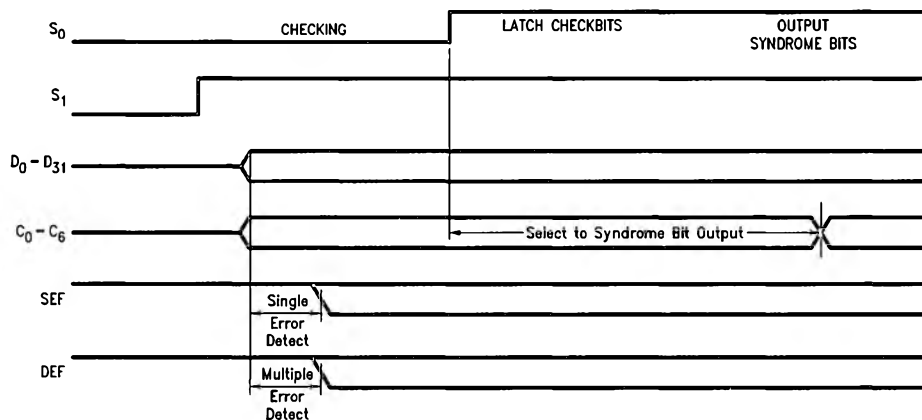
Timing Waveforms

SEF = H
DEF = H



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FIGURE 420-a.



TL/F/9542-6

FIGURE 420-b.

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

