October 1999

National Semiconductor

54FCT138
1-of-8 Decoder/Demultiplexer

General Description

The FCT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three FCT138 devices or a 1-of-32 decoder using four FCT138 devices and one inverter.

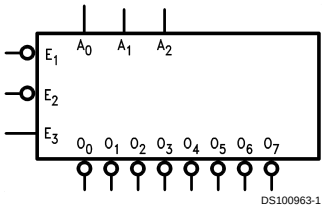
Features

- Demultiplexing capability
- Multiple input enable for easy expansion
- Active LOW mutually exclusive outputs
- Outputs sink capability of 32mA, source capability of 12mA
- TTL input and output level compatible
- CMOS power consumption
- Standard Microcircuit Drawing (SMD) 5962-8765401

Ordering Code

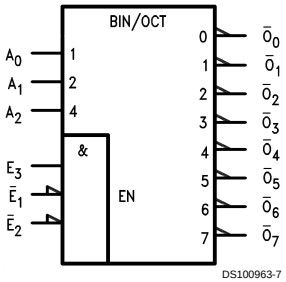
Military	Package Number	Package Description
54FCT138DMQB	J16A	16-Lead Ceramic Dual-In-Line
54FCT138FMQB	W16A	16-Lead Cerpack
54FCT138LMQB	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Logic Symbols



DS100963-1

IEEE/IEC

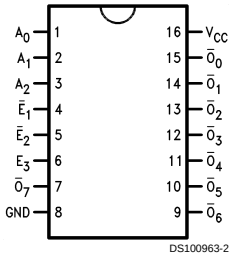


DS100963-7

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

Connection Diagrams

Pin Assignment for DIP and Flatpak



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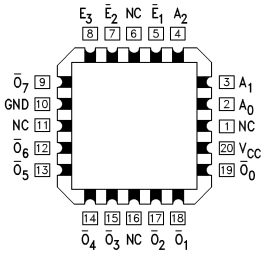
Pin Assignment for LCC



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FACT® is a registered trademark of Fairchild Semiconductor Corporation.

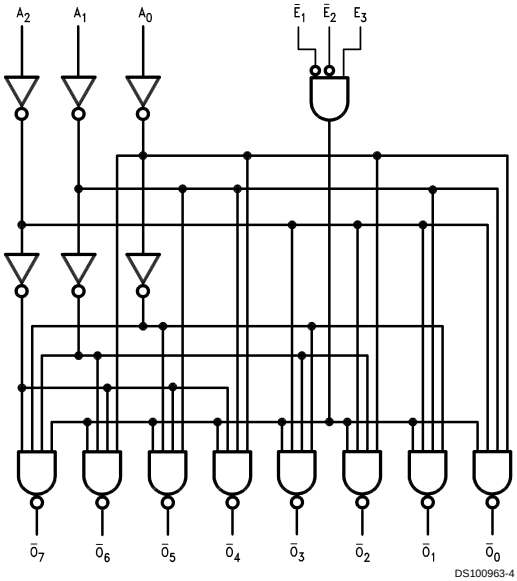
Functional Description

The FCT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_7$). The FCT138 features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four FCT138 devices and one inverter (see *Figure 1*). The FCT138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagram (Continued)

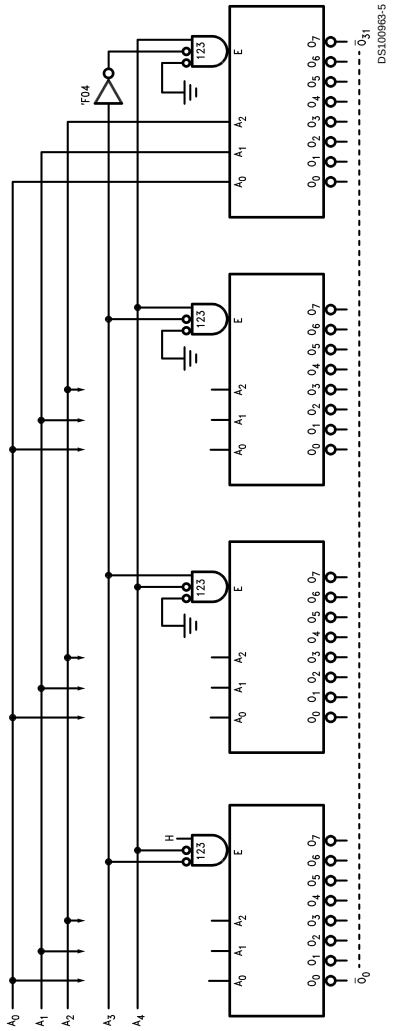


FIGURE 1. Expansion to 1-of-32 Decoding

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (Note 1)	−0.5V to +7.0V
Input Current (Note 1)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	Twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'FCT Family Devices

Symbol	Parameter		FCT138 Min	FCT138 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54FCT	4.3		V	Min	I_{OH} = −300 µA
		54FCT	2.4				I_{OH} = −12 mA
V_{OL}	Output LOW Voltage	54FCT		0.2	V	Min	I_{OL} = 300 µA
		54FCT		0.5			I_{OL} = 32 mA
I_{IH}	Input HIGH Current			5	µA	Max	V_{IN} = V_{CC}
I_{IL}	Input LOW Current			−5	µA	Max	V_{IN} = 0.0V
I_{OS}	Output Short-Circuit Current			-60	mA	Max	V_{OUT} = 0.0V
I_{CCQ}	Quiescent Power Supply Current			1.5	mA	Max	V_{IN} < 0.2V or V_{IN} 5.3V, V_{CC} = 5.5V
ΔI_{CC}	Quiescent Power Supply Current			2.0	mA	Max	V_I = 3.4V, V_{CC} = 5.5V
I_{CCD}	Dynamic I_{CC}			0.4	mA/ MHz	Max	Outputs Open, V_{CC} = 5.5V, V_{IN} 5.3V or V_{IN} < 0.2V, One Bit Toggling, 50% Duty Cycle, $\overline{OE}$ = GND, LE = V_{CC}
I_{CCT}	Total Power Supply Current			5.5	mA	Max	Outputs Open, f_{CP} = 10 MHz, V_{CC} = 5.5V, V_{IN} 5.3V or V_{IN} < 0.2V, One Bit Toggling, 50% Duty Cycle, $\overline{OE}$ = GND, LE = V_{CC}

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

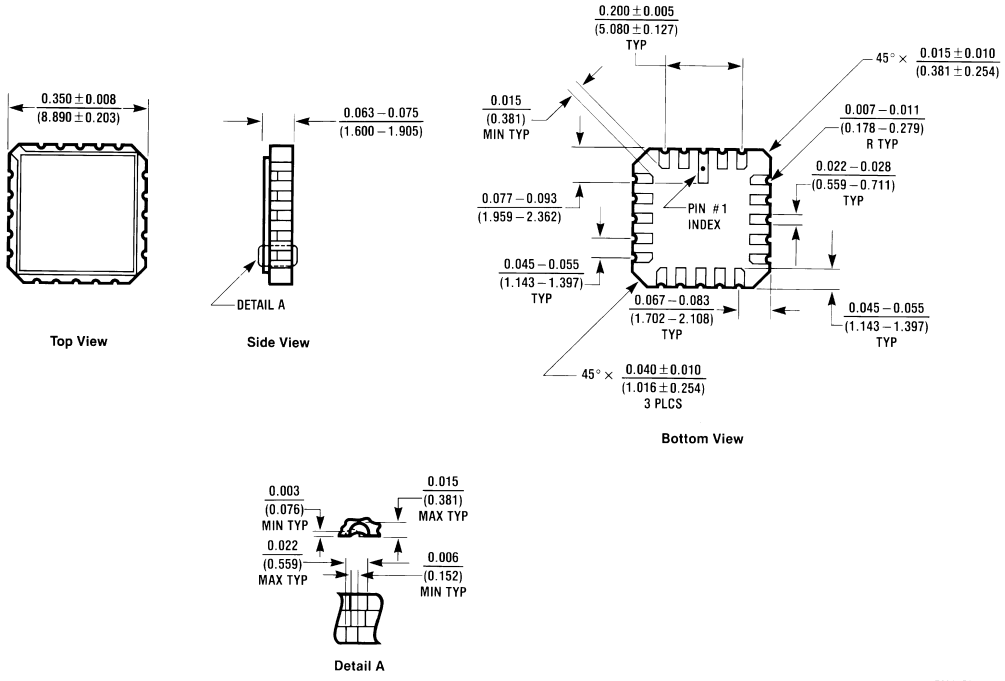
Symbol	Parameter	V_{CC} (V) (Note 4)	54FCT T_A = −55°C to +125°C C_L = 50 pF		Units	Fig. No.
			Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.0	12.0	ns	
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.0	12.0	ns	
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.0	12.5	ns	
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.0	12.5	ns	
t_{PLH}	Propagation Delay E_3 to $\overline{O}$ n	5.0	1.0	12.5	ns	
t_{PHL}	Propagation Delay E_3 to $\overline{O}$ n	5.0	1.0	12.5	ns	

Note 4: Voltage Range 5.0 is 5.0V ±0.5V

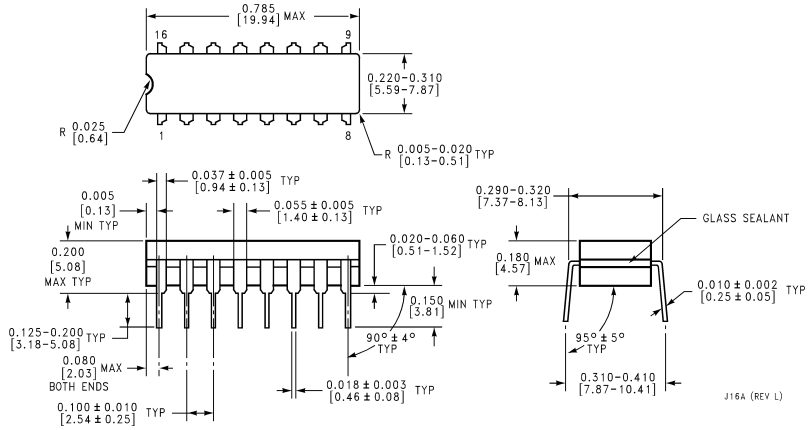
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	60.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

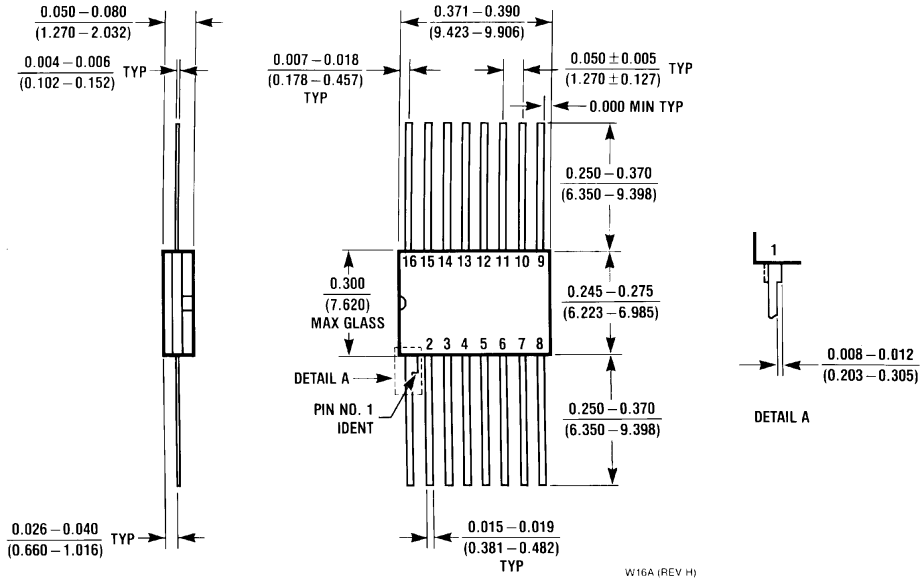


20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



16 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16 Lead Ceramic Flatpak (F)
NS Package Number W16A

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