National Semiconductor

August 1998

# 54FCT273
# Octal D-Type Flip-Flop

## General Description

The 'FCT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

## Features

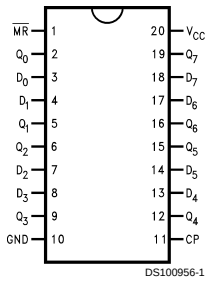
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous Master Reset
- See 'FCT377 for clock enable version
- See 'FCT373 for transparent latch version
- See 'FCT374 for TRI-STATE® version
- Output sink capability of 32 mA, source capability of 12 mA
- TTL input and output level compatible
- CMOS power consumption
- Standard Microcircuit Drawing (SMD) 5962-8765601

## Ordering Code

| Military | Package Number | Package Description |
|---|---|---|
| 54FCT273DMQB | J20A | 20-Lead Ceramic Dual-In-Line |
| 54FCT273FMQB | W20A | 20-Lead Cerpack |
| 54FCT273LMQB | E20A | 20-Lead Ceramic Leadless Chip Carrier, Type C |

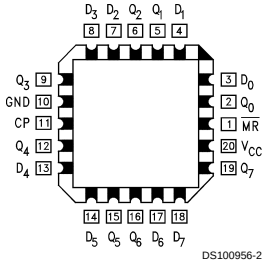
## Connection Diagrams

**Pin Assignment for DIP and Flatpack**




DS100956-1

**Pin Assignment for LCC**




DS100956-2

| Pin Names | Description |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| $\overline{MR}$ | Master Reset (Active LOW) |
| CP | Clock Pulse Input (Active Rising Edge) |
| $Q_0$–$Q_7$ | Data Outputs |

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

© 1998 National Semiconductor Corporation 

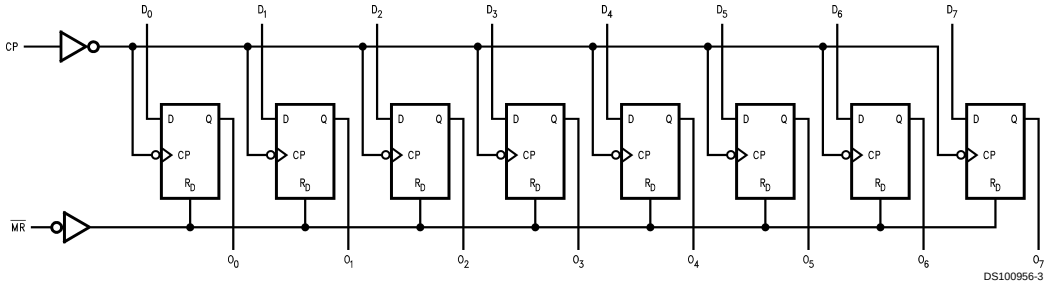
## Truth Table

H = HIGH Voltage Level steady state
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Immaterial
N = LOW-to-HIGH clock transition

## Mode Select-Function Table

| Operating Mode | Inputs | | | Output |
|---|---|---|---|---|
| | $\overline{MR}$ | CP | $D_n$ | $Q_n$ |
| Reset (Clear) | L | X | X | L |
| Load “1” | H | N | h | H |
| Load “0” | H | N | l | L |

## Logic Diagram




DS100956-3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Storage Temperature | −65˚C to +150˚C |
| Ambient Temperature under Bias | −55˚C to +125˚C |
| Junction Temperature under Bias | |
| Ceramic | −55˚C to +175˚C |
| $V_{CC}$ Pin Potential to | |
| Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 2) | −0.5V to +7.0V |
| Input Current (Note 2) | −30 mA to +5.0 mA |
| Voltage Applied to Any Output | |
| in the Disabled or | |
| Power-Off State | −0.5V to +4.75V |
| in the HIGH State | −0.5V to $V_{CC}$ |
| Current Applied to Output | |
| in LOW State (Max) | twice the rated $I_{OL}$ (mA) |
| DC Latchup Source Current | −500 mA |
| (Across Comm Operating Range) | |
| Over Voltage Latchup | $V_{CC}$ + 4.5V |

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | |
| Military | −55˚C to +125˚C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

| Symbol | Parameter | | FCT240 Min | FCT240 Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | V | | Recognized HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | | Recognized LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 54FCT | 4.3 | | V | Min | $I_{OH}$ = −300 uA |
| | | 54FCT | 2.4 | | V | Min | $I_{OH}$ = −12 mA |
| $V_{OL}$ | Output LOW Voltage | 54FCT | | 0.2 | V | Min | $I_{OL}$ = 300 µA |
| | | 54FCT | | 0.5 | V | Min | $I_{OL}$ = 32 mA |
| $I_{IH}$ | Input HIGH Current | | | 5 | µA | Max | $V_{IN}$ = 5.5V |
| $I_{IL}$ | Input LOW Current | | | −5 | µA | Max | $V_{IN}$ = 0.0V |
| $I_{OS}$ | Output Short-Circuit Current | | | −60 | mA | Max | $V_{OUT}$ = 0.0V |
| $I_{CCQ}$ | Power Supply Current | | | 1.5 | mA | Max | $V_{IN}$ = 0.2V or $V_{IN}$ = 5.3V |
| $\Delta I_{CC}$ | Power Supply Current | | | 2.0 | mA | Max | $V_{IN}$ = 3.4V |
| $I_{CCT}$ | Total Power Supply Current | | | 6.0 | mA | Max | $V_{IN}$ = 3.4V or $V_{IN}$ = GND, $\overline{OE}$ = GND, $f_i$ = 10Mhz, outputs open, one bit toggling - 50% duty cycle |
| | | | | 4.0 | mA | Max | $V_{IN}$ = 5.3V or $V_{IN}$ = 0.2V, $\overline{OE}$ = GND, $f_i$ = 10Mhz, outputs open, one bit toggling - 50% duty cycle |
| $I_{CCD}$ | Dynamic $I_{CC}$ | | | 0.25 | mA/MHz | Max | Outputs Open, $\overline{OE}$ = GND, One Bit Toggling, 50% Duty Cycle |

## AC Electrical Characteristics

| Symbol | Parameter | 54FCT $T_A$ = −55˚C to +125˚C, $V_{CC}$ = 4.5V to 5.5V, $C_L$ = 50 pF Min | 54FCT Max | Units | Fig. No. |
|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay | 2.0 | 15.0 | ns | *Figures 2, 5* |
| $t_{PHL}$ | CP to $O_n$ | 2.0 | 15.0 | | |
| $t_{PHL}$ | Propagation Delay $\overline{MR}$ to $O_n$ | 2.0 | 15.0 | ns | *Figures 2, 5* |

## AC Operating Requirements

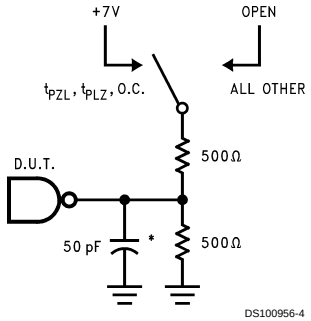
| Symbol | Parameter | 54FCT $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF | | Units | Fig. No. |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_s(H)$<br>$t_s(L)$ | Setup Time, HIGH<br>or LOW $D_n$ to CP | 3.5<br>3.5 | | ns | *Figure 6* |
| $t_h(H)$<br>$t_h(L)$ | Hold Time, HIGH<br>or LOW $D_n$ to CP | 2.5<br>2.5 | | ns | *Figure 6* |
| $t_w(H)$<br>$t_w(L)$ | Pulse Width, CP,<br>HIGH or LOW | 7.0<br>7.0 | | ns | *Figure 2* |
| $t_w(L)$ | Master Reset Pulse<br>Width, LOW | 7.0 | | ns | *Figure 2* |
| $t_{REC}$ | Recovery Time<br>$\overline{MR}$ to CP | 5.0 | | ns | *Figure 6* |

## Capacitance

| Symbol | Parameter | Max | Units | Conditions $T_A = 25^\circ C$ |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 10 | pF | $V_{CC} = 0V$ |
| $C_{OUT}$ (Note 3) | Output Capacitance | 12 | pF | $V_{CC} = 5.0V$ |

**Note 3:** $C_{OUT}$ is measured at frequency f = 1 MHz, per MIL-STD-833B, Method 3012.

## AC Loading




*Includes jig and probe capacitance

**FIGURE 1. Standard AC Test Load**

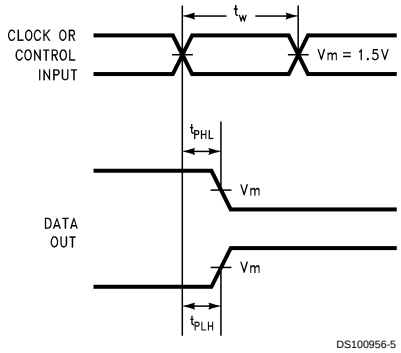



**FIGURE 2. Propagation Delay, Pulse Width Waveforms**

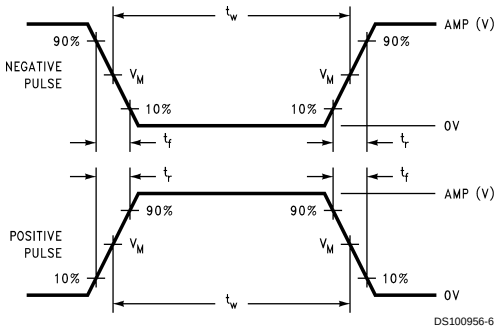



**FIGURE 3. $V_M$ = 1.5V Input Pulse Requirements**

| Amplitude | Rep. Rate | $t_w$ | $t_r$ | $t_f$ |
|---|---|---|---|---|
| 3.0V | 1 MHz | 500 ns | 2.5 ns | 2.5 ns |

**FIGURE 4. Test Input Signal Requirements**

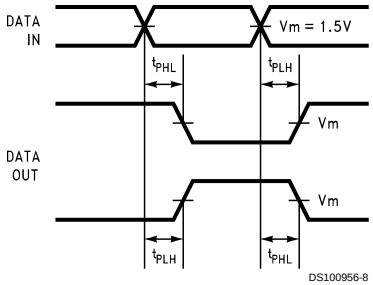



**FIGURE 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**

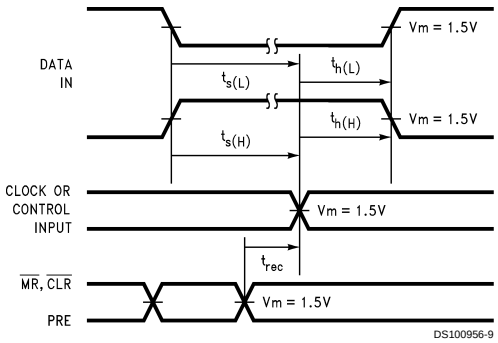
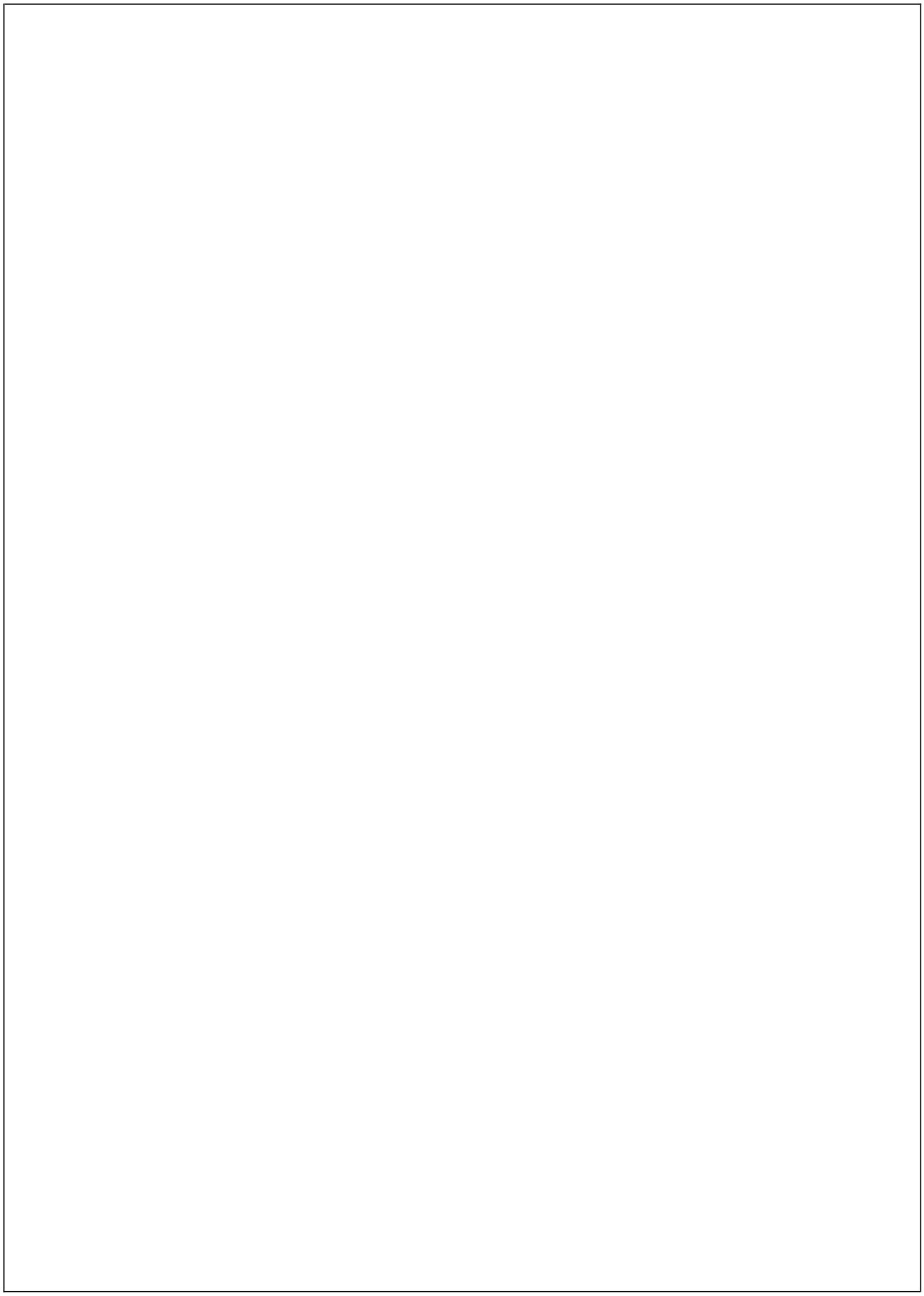
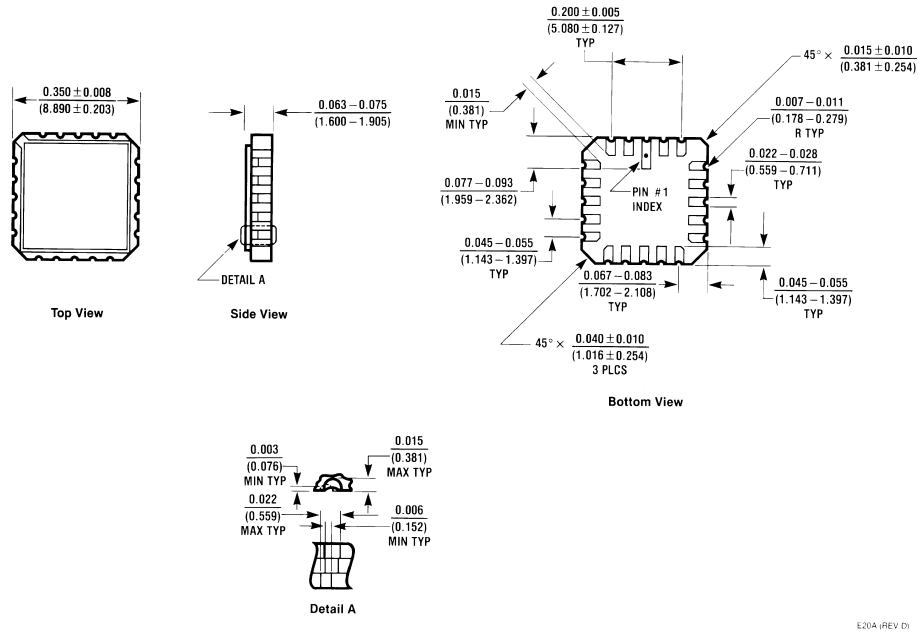


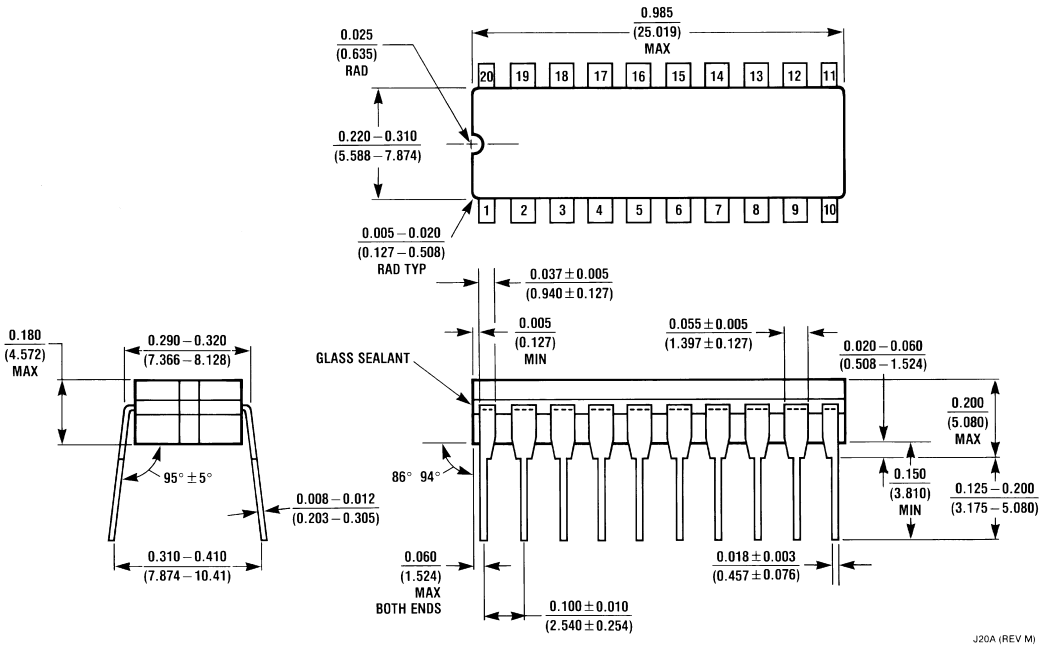

**FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms**



## Physical Dimensions inches (millimeters) unless otherwise noted

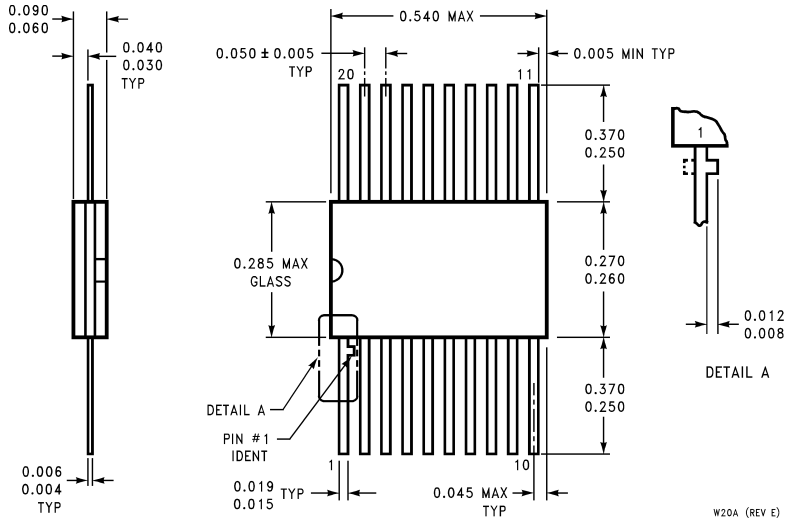



**20-Terminal Ceramic Chip Carrier (L)**
**NS Package Number E20A**




**20-Lead Ceramic Dual-In-Line (D)**
**NS Package Number J20A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead Ceramic Flatpak (F)**
**NS Package Number W20A**

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**National Semiconductor Corporation**
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

**National Semiconductor Europe**
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

**National Semiconductor Asia Pacific Customer Response Group**
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

**National Semiconductor Japan Ltd.**
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.