National Semiconductor

54FCT377/74FCT377
Octal D Flip-Flop with Clock Enable

General Description

The FCT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

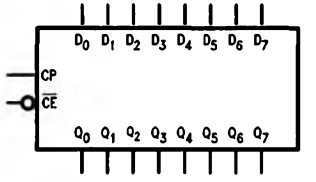
FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 54FCT/74FCT377 is pin and functionally equivalent to IDT 54FCT/74FCT377
- Ideal for addressable register applications
- Clock enables for address and data synchronization applications
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (com), 32 mA (mil)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD 883 and Standard Military Drawing # 5962-87627

Ordering Code: See Section 8

Logic Symbols



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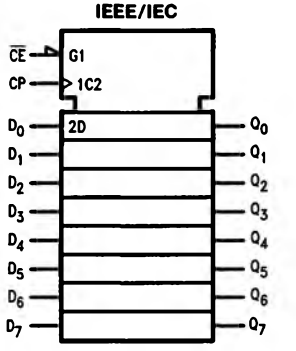

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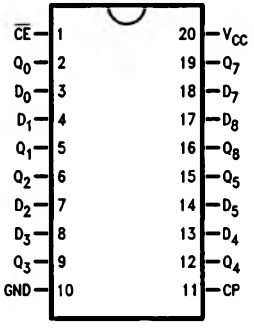
Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0–Q_7	Data Outputs
CP	Clock Pulse Input

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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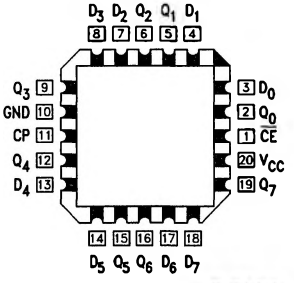
Pin Assignment for LCC



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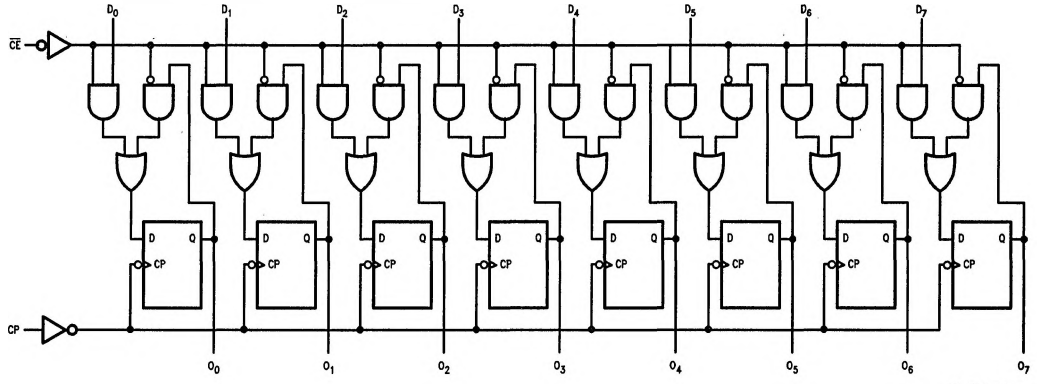
Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D_n	Q_n
Load '1'	⌐	L	H	H
Load '0'	⌐	L	L	L
Hold (Do Nothing)	⌐	H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCT: −0.5V to +7.0V
- 74FCT: −0.5V to +7.0V

Temperature Under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0	μA	V_{CC} = Max	$V_I = V_{CC}$
				5.0			V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2)
				−5.0			V_I = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC}	V_{CC}			V_{CC} = Min; $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA
		2.4	4.3				I_{OH} = −12 mA (Mil)
		2.4	4.3				I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND	0.2		V_{CC} = Min; $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA
			0.3	0.5			I_{OL} = 32 mA (Mil)
			0.3	0.5			I_{OL} = 48 mA (Com)

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ $f_I = 0$	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.30	mA/MHz	V_{CC} = Max Outputs Open $\overline{CE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open f_{CP} = 10 MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0		$\overline{CE}$ = GND f_I = 5 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	9.0		(Note 5) V_{CC} = Max Outputs Open f_{CP} = 10 MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8		$\overline{CE}$ = GND f_I = 2.5 MHz Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs HIGH

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.4 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT T_A = 25°C V_{CC} = 5.0V	74FCT T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		54FCT T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF		Units	Fig. No.
		Typ	Min (Note)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_P to $\overline{O}_n$	7.0	2.0	13.0	2.0	13.0	ns	2-8
t_{SU}	Set Up Time HIGH or LOW D_n to C_P	1.0	2.5		4.0		ns	2-10
t_H	Hold Time HIGH or LOW D_n to C_P	1.0	2.0		2.0		ns	2-10
t_{SU}	Set Up Time HIGH or LOW $\overline{CE}$ to C_P	1.5	4.0		4.5		ns	2-10
t_H	Hold Time HIGH or LOW $\overline{CE}$ to C_P	3.0	1.5		2.0		ns	2-10
t_W	Clock Pulse Width, LOW	4.0	7.0		7.0		ns	2-9

Note: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance T_A = +25°C, f = 1.0 MHz

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.
C_{OUT} for 74FCT only.