National Semiconductor

54FCT/74FCT533
Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 'FCT533 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state. FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance. FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance. The 'FCT533 is the same as the 'FCT373, except that the outputs are inverted.

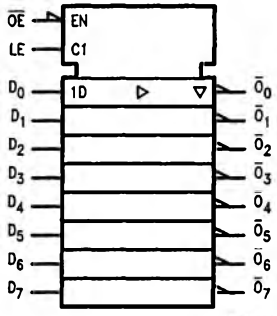
Features

- NSC 54FCT/74FCT533 is pin and functionally equivalent to IDT 54FCT/74FCT533
- TRI-STATE outputs for bus interfacing
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- ESD immunity 4 kV typ
- Military product compliant to MIL-STD 883 and Standard Military Drawing #5962-88651

Ordering Code: See Section 8

Logic Symbols

IEEE/IEC



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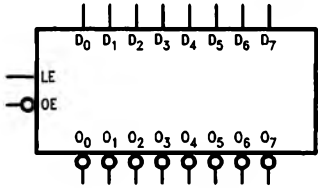

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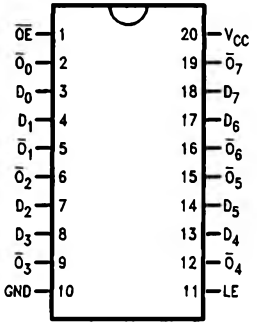
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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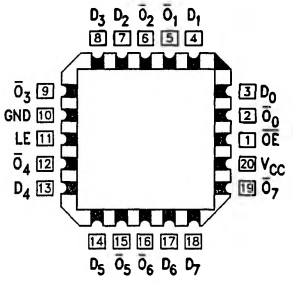
Pin Assignment for LCC



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Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{O}_0$–$\overline{O}_7$	Complementary TRI-STATE Outputs

Function Table

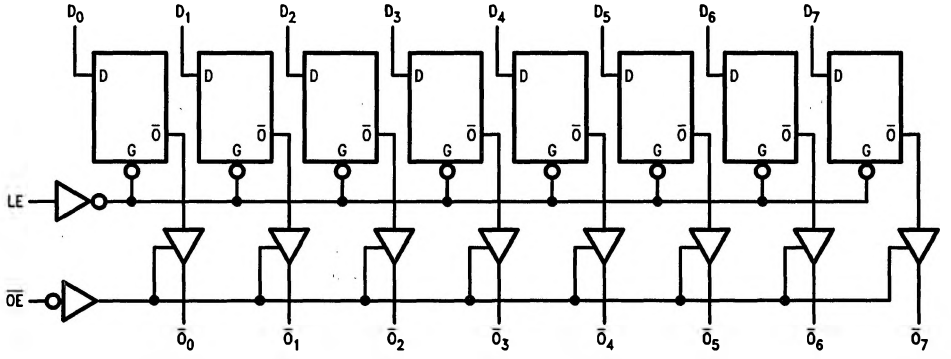
Inputs			Output
LE	$\overline{OE}$	D	$\overline{O}$
H	L	H	L
H	L	L	H
L	L	X	$\overline{O}_n$
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Logic(0) or logic(1) must be valid Input Level
O_n = Previous $\overline{O}_n$ before high to low transition of latch enable.

Functional Description

The 'FCT533 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent and the latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW the latch contents are presented inverted at the outupts $\overline{O}_7$–$\overline{O}_0$. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Voltage with respect to GND (V_{TERM})
- 54FCT: −0.5V to +7.0V
- 74FCT: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C to +125°C.

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum HIGH Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_{IN} = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC}	V_{CC}			V_{CC} = Min; $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA
		2.4	4.3				I_{OH} = −12 mA (Mil)
		2.4	4.3				I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND	0.2		V_{CC} = Min; $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA
			0.3	0.50			I_{OL} = 32 mA (Mil)
			0.3	0.50			I_{OL} = 48 mA (Com)

DC Characteristics for FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C to +125°C. (Continued)

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.45	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} f_I = 10 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5			V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on LE Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz. Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0V$	T_A, V_{CC} = Com $R_L = 500\Omega$ $C_L = 50$ pF		T_A, V_{CC} = Mil $R_L = 500\Omega$ $C_L = 50$ pF			
		Typ	Min (Note 1)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	6.0	1.5	10.0	1.5	8.5	ns	2–8
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	9.0	2.0	13.0	2.0	9.5	ns	2–8
t_{PZH} t_{PZL}	Output Enable Time	8.0	1.5	11.0	1.5	12.5	ns	2–11
t_{PHZ} t_{PLZ}	Output Disable Time	6.0	1.5	7.0	1.5	8.5	ns	2–11
t_S	Set Up Time High or Low D_n to LE	1.0	2.0		2.0		ns	2–10
t_H	HOLD Time High or Low D_n to LE	1.0	1.5		3.0		ns	2–10
t_W	LE Pulse Width High or Low	5.0	6.0		6.0		ns	2–9

Note 1: Minimum limits are guaranteed but not tested on Propagation Delays

Capacitance ($T_A = +25C, f = 1.0$ MHz)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{in}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{out}	Output Capacitance	8	12	pF	$V_{out} = 0V$

Note: This parameter is measured at characterization but not tested
C_{OUT} for 74FCT only.