## 54LCX16374

54LCX16374 Low Voltage 16-Bit D Flip-Flop with 5V Tolerant Inputs and Outputs



Literature Number: SNOS488A



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# Low Voltage 16-Bit D Flip-Flop with 5V Tolerant Inputs and Outputs

#### **General Description**

The LCX16374 contains sixteen non-inverting D flip-flops with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable  $(\overline{OE})$  are common to each byte and can be shorted together for full 16-bit operation.

The LCX16374 is designed for low voltage (3.3V)  $\rm V_{\rm CC}$  applications with capability of interfacing to a 5V signal environment.

The LCX16374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

#### **Features**

- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V-3.6V V<sub>CC</sub> supply operation
- ±24 mA output drive
- Implements patented noise/EMI reduction circuitry
- Functionally compatible with the 54 series 16374
- ESD performance:

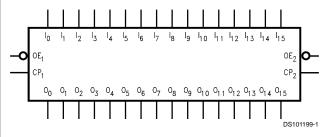
Human body model > 2000V Machine model > 200V

■ Standard Microcircuit Drawing (SMD) 5962-99535

## **Ordering Code**

Order Number	Package Number	Package Description
54LCX16374W-QML	WA48A	48-Lead Ceramic Flatpack

#### **Logic Symbol**



### **Pin Descriptions**

Pin	Description	
Names		
ŌĒn	Output Enable Input (Active Low)	
CP <sub>n</sub>	Clock Pulse Input	
I <sub>0</sub> -I <sub>15</sub>	Inputs	
O <sub>0</sub> -O <sub>15</sub>	Outputs	

#### **Connection Diagram**

# 

Pin Assignment for



TRI-STATE® is a registered trademark of National Semiconductor Corporation.

#### **Functional Description**

The LCX16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs andTRI-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP<sub>n</sub>) transition. With the Output Enable  $(\overline{\text{OE}}_n)$  LOW, the contents of the flip-flops are available at the outputs. When  $\overline{\text{OE}}_n$  is HIGH, the outputs go to the high impedance state. Operation of the OE<sub>n</sub> input does not affect the state of the flip-flops.

Inputs			Outputs
CP <sub>1</sub>	$\overline{OE}_1$ $I_0-I_7$		O <sub>0</sub> -O <sub>7</sub>
	L	Н	Н
	L	L	L
L	L	X	O <sub>o</sub>
X	Н	X	Z

Inputs			Outputs	
CP <sub>2</sub>	OE <sub>2</sub> I <sub>8</sub> -I <sub>15</sub>		O <sub>8</sub> -O <sub>15</sub>	
	L	Н	Н	
	L	L	L	
L	L	X	O <sub>o</sub>	
X	Н	X	Z	

H = High Voltage Level

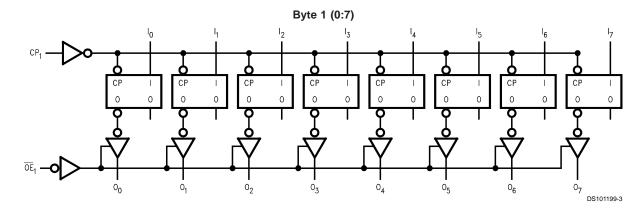
L = Low Voltage Level

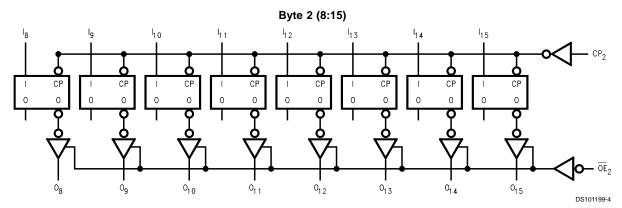
X = Immaterial

Z = High Impedance

 $O_0$  = Previous  $O_0$  before HIGH to LOW of CP

#### **Logic Diagrams**





Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V<sub>CC</sub>) -0.5V to +7.0VDC Input Voltage (V<sub>I</sub>) -0.5V to +7.0V

DC Input Diode Current (I<sub>IK</sub>)

 $V_1 < GND$ -50 mA

DC Output Diode Current (IOK)

 $V_{O} < GND$ -50mA  $V_O \ge V_{CC}$ +50mA

DC Output Voltage (Vo) (Note

2)

Output in High or Low State -0.5V to  $V_{\rm CC}$  + 0.5V Output in TRI-STATE -0.5V to 7.0V

DC Output Source or Sink

±50mA Current (I<sub>O</sub>)

DC V<sub>CC</sub> or Ground Current ±100mA

Storage Temperature Range

 $(T_{STG})$ -65°C to +150°C

Power Dissapation 750mW Junction Temperature (T<sub>1</sub>) 175°C

#### **Recommended Operating** Conditions (Note 3)

Supply Voltage (V<sub>CC</sub>)

2.0V to 3.6V Operating 1.5V to 3.6V Data Retention Input Voltage (V<sub>I</sub>) 0V to 5.5V

Output Voltage (V<sub>O</sub>)

High or Low State 0V to  $V_{\text{CC}}$ TRI-STATE 0V to 5.5V Operating Temperature (T<sub>A</sub>)  $-55^{\circ}C$  to

+125°C

Minimum Input Edge Rate (Δt/ΔV)

 $V_{IN}$  from 0.8V to 2.0V,  $V_{CC} = 3.0V$ 0ns/V to 10ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: IO Absolute Maximum Rating must be observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

#### **DC Electrical Characteristics**

Symbol	Parameter	Conditions	V <sub>cc</sub>	$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$		Units
			(V)	Min	Max	1
V <sub>IH</sub>	HIGH Level Input Voltage		2.7-3.6	2.0		V
V <sub>IL</sub>	LOW Level Input Voltage		2.7-3.6		0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -100 μA	2.7-3.6	V <sub>CC</sub> - 0.2		V
		I <sub>OH</sub> = -12 mA	2.7	2.2		V
		I <sub>OH</sub> = -12 mA	3.0	2.4		V
		$I_{OH} = -24 \text{ mA}$	3.0	2.2		V
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	2.7-3.6		0.2	V
		I <sub>OL</sub> = 12 mA	2.7		0.4	V
		I <sub>OL</sub> = 24 mA	3.0		0.55	V
I <sub>I</sub>	Input Leakage Current	$0 \le V_1 \le 5.5V$	2.7-3.6		±5.0	μΑ
l <sub>oz</sub>	3-STATE Output Leakage	0 ≤ V <sub>O</sub> ≤ 5.5V	2.7-3.6		±5.0	μΑ
		$V_I = V_{IH} \text{ or } V_{IL}$				
I <sub>OFF</sub>	Power-Off Leakage Current	$V_{I}$ or $V_{O} = 5.5V$	0		10	μΑ
I <sub>cc</sub>	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7-3.6		20	μΑ
		$3.6V \le V_1, V_0 \le 5.5V$	2.7-3.6		±20	μΑ
$\Delta I_{CC}$	Increase in I <sub>CC</sub> per Input	$V_{IH} = V_{CC} - 0.6V$	2.7-3.6		500	μA

## **AC Electrical Characteristics**

	Parameter	$T_A = -55$ °C to +125°C, $C_L = 50$ pF, $R_L = 500$ $\Omega$				
Symbol		$V_{CC} = 3.3V \pm 0.3V$		V <sub>CC</sub> = 2.7V		Units
		Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	200		200		MHz
t <sub>PHL</sub>	Propagation Delay	0.5	6.5	1.0	7.0	ns
t <sub>PLH</sub>	CP to O <sub>n</sub>	0.5	6.5	1.0	7.0	
t <sub>PZL</sub>	Output Enable Time	0.5	6.5	1.0	7.0	ns
t <sub>PZH</sub>		0.5	6.5	1.0	7.0	
t <sub>PLZ</sub>	Output Disable Time	1.0	6.5	1.0	7.0	ns
t <sub>PHZ</sub>		1.0	6.5	1.0	7.0	
t <sub>S</sub>	Setup Time	3.5		3.5		ns
t <sub>H</sub>	Hold Time	2.0		2.0		ns
t <sub>w</sub>	Pulse Width	4.0		4.0		ns
t <sub>OSHL</sub>	Output to Output Skew (Note 4)		1.0		1.0	ns
toslh			1.0		1.0	

Note 4: Skew is defined as the absolute value of the difference between the actual propagation delay for any two seperate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

# **Dynamic Switching Characteristics**

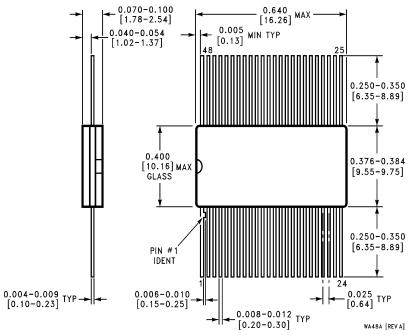
Symbol	Parameter	Conditions	V <sub>cc</sub> (V)	T <sub>A</sub> = 25°C Max	Units
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	3.3	1.2	V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	3.3	-1.1	V

# Capacitance

Symbol	Parameter	Conditions	Max	Units
C <sub>IN</sub>	Input Capacitance	$V_{CC}$ = Open, $V_{I}$ = 0V or $V_{CC}$	10	pF
C <sub>OUT</sub>	Output Capacitance	$V_{CC} = 3.3V$ , $V_{I} = 0V$ or $V_{CC}$	12	pF
C <sub>PD</sub>	Power Dissipation Capacitance	$V_{CC} = 3.3V$ , $V_{I} = 0V$ or $V_{CC}$ , $f = 10$ MHz	40	pF

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#### Physical Dimensions inches (millimeters) unless otherwise noted



#### 48-Lead Ceramic Flatpack Package Number WA48A

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