

54S/74S113

54LS/74LS113

DUAL JK EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The '113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

TRUTH TABLE

INPUTS		OUTPUT
@ t_n	@ $t_n + 1$	
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

Asynchronous Input:

LOW input to $\bar{S}_D$ sets Q to HIGH level
Set is independent of clock

t_n = Bit time before clock pulse.
 $t_n + 1$ = Bit time after clock pulse.
 H = HIGH Voltage Level
 L = LOW Voltage Level

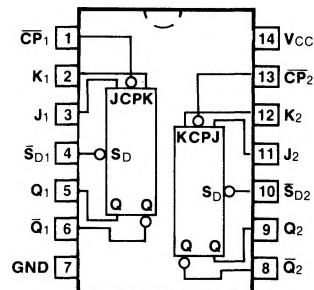
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0 \text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74S113PC, 74LS113PC		9A
Ceramic DIP (D)	A	74S113DC, 74LS113DC	54S113DM, 54LS113DM	6A
Flatpak (F)	A	74S113FC, 74LS113FC	54S113FM, 54LS113FM	3I

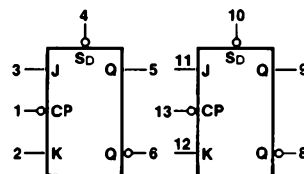
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J ₁ , J ₂ , K ₁ , K ₂	Data Inputs	1.25/1.0	0.5/0.25
$\bar{CP}_1$, $\bar{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	2.5/2.5	2.0/0.5
$\bar{S}_{D1}$, $\bar{S}_{D2}$	Direct Set Inputs (Active LOW)	2.5/4.375	1.5/0.5
Q ₁ , Q ₂ , $\bar{Q}_1$, $\bar{Q}_2$	Outputs	25/12.5	10/5.0 (2.5)

CONNECTION DIAGRAM PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 14
 GND = Pin 7

